

Application of PMA Towards Moderating the Charge Storage Capability of MIS Memory Cell Based on PECVD Deposited Silicon Nitride Thin Films

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Received 13.07.2007

Abstract

A memory capacitor formed from Al/Si₃N₄/Si was prepared by means of trapping and de trapping mechanism of the dielectric films. Charge trapping and interface state characteristics of silicon nitride (Si₃N₄) films deposited by standard plasma enhanced chemical vapor deposition technique were investigated. High frequency capacitance-voltage (C-V), conductance-voltage (G-V) and current voltage (I-V) measurements were carried out at various temperatures on metal-oxide-semiconductor capacitors, for as-deposited samples, post metallization annealed (PMA) at 400 °C and 600 °C samples. The electrically measured characteristics indicate the shift in flat band voltage V_{FB} in silicon nitride (Si₃N₄) was initially much higher in the as-deposited samples. This is attributed to its high density of interface traps and higher capability to store the charges in the deep traps for the application of non volatile memory devices. An enlarged memory window in CV characteristics was observed in memory operations, due to the higher density of traps in silicon–nitride films. Following post-metallization annealing there is significant shift in flat band voltage due to moderation of trapping and de-trapping sites at the interface of thin films; and with this, a new method of post metallization annealing (PMA) is proposed to moderate the charge storage capability of metal insulator semiconductor (MIS) memory cell. This behavior of as-deposited Al/Si₃N₄/Si MIS structure, and of low temperature post metallization annealed samples, suggests the behavior is due to the holes trapping and de-trapping mechanism at the Al/Si₃N₄/Si interface, not due to ionic charge displacement. The larger memory window indicated by the width of hysteresis and longer retention time in the memory operations are discussed in terms of trap-assisted charging / discharging mechanisms.

Key Words: PECVD, Nitride films, C-V, G-V,I-V, P M A, hysteresis and memory window.

1. Introduction

Nitride/silicon interface based nonvolatile memory devices have received much attention recently as a result of continued scaling of MOSFETs devices. Therefore, to reduce the leakage current of memory devices, high-K dielectrics such as yttrium oxide (Y₂O₃), hafnium oxide (HfO₂) and zirconium oxide (ZrO₂) have been under intense investigation recently for replacing conventional SiO₂ as the gate dielectric from metal-oxide-semiconductor (MOS) memory device application [1]. In spite of their excellent dielectric properties, these materials are not compatible with silicon processing and therefore they have poor interface properties. The

key issues for memory devices are charge trapping and de-trapping, specifically for the bulk and interface charges of the MIS devices [2]. Even though significant efforts of many workers have been dedicated to the investigation of silicon nitride based MIS memory systems, due to its higher surface roughness and interface traps and its ability to suppress boron penetration from p^+ polysilicon gate to Si substrate [3, 4]. The nitride based MIS system is commonly known to have a higher density of localized defect sites, but discharge properties are roughly similar to the Si-SiO₂ system [5]. Therefore, a nominal number of trap sites from nitride on the interface may contribute in charge retention, but not degrade the device reliability or performance considerably [6]. Silicon nitride films can be grown or deposited by a number of techniques. Nitridation of SiO₂ by standard high-temperature or rapid thermal processing is extensively used. Other standard alternatives to the nitrided oxide process are low-pressure chemical vapor deposition (LPCVD) and plasma-enhanced chemical vapor deposition (PECVD) [7–9]; these processes avoid a high thermal budget and are compatible with the requirements of advanced submicron device technology.

2. Experimental

P-type silicon wafers with <100> orientation and 15–20 Ω·cm resistivity were used for the fabrication of MIS capacitors. The silicon wafers were cleaned with the standard RCA cleaning technique. After drying in the nitrogen ambient atmosphere, wafers were loaded into the PECVD system of the Plasma Lab Technology at Central Electronic Engineering Research Institute (CEERI), Pilani, India. During deposition the temperature measured at the sample holder was 300 °C. The background pressure in the reaction chamber was below 0.2 Torr. The silicon nitride layer was deposited using the reacting species nitrogen (N₂) 30 sccm, silane (SiH₄) 80 sccm and ammonia (NH₃) 25 sccm were introduced directly into the resonance zone at pressure 0.4 Torr. The plasma power was selected to be at 120 W for nitride deposition. The thickness of the deposited silicon nitride layers were 40 nm as measured via an ellipsometer at CEERI, Pilani-India. A 300 nm aluminum (Al) film was deposited over Si₃N₄ layers using a thermal evaporation system with in-situ thickness monitor at the Electronic Science Department, Kurukshetra University, Kurukshetra (India). The gate electrodes of area 1.8×10^{-2} cm² were defined by standard photolithography and chemical etching techniques. The samples were subjected to a post-metallization annealing in dry nitrogen ambient at 400 °C and 600 °C for 30 min to investigate the effect of post-metallization on interface state density. The MIS capacitors were electrically characterized at room temperature by capacitance-voltage (C-V) and conductance-voltage (G-V) method at 1 MHz frequency using the Keithley Model 82-DOS Simultaneous C-V system and current-voltage (I-V); and measurement for the study of the Fowler-Nordheim tunneling mechanism conducted with a Keithley 2602 Source Meter.

3. Results and Discussion

3.1. Effect of PMA on C-V hysteresis

Figure 1 show the forward and reverse C-V curves for as-deposited samples obtained when the gate voltage was first swept from –10V to +10V (accumulation to inversion, forward sweep) and then from +10V to –10V (inversion to accumulation, reverse sweep) for the nitride (Si₃N₄) based MIS structure. The as-deposited samples with nitride as the dielectric material show significant hysteresis of ~7 V and a large flat band voltage shift in the capacitance-voltage characteristics as shown in curves ‘g’ and ‘h’ of Figure 1. For the calculation of flat-band capacitance C_{FB} equations (1) and (2) were used.

The C_{FB} is calculated as

$$C_{FB} = \frac{C_{ox}\epsilon_s A / (1 \times 10^{-4})(\lambda)}{(1 \times 10^{-12})(C_{ox}) + \epsilon_s A / (1 \times 10^{-4})(\lambda)} \quad (1)$$

$$\lambda = (1 \times 10^4) \left(\frac{\varepsilon_s kT}{q^2 N_x} \right)^{1/2}. \quad (2)$$

C_{FB} , C_{ox} , ε_s , A , λ , kT , q and N_x are the flatband capacitance (pF), oxide capacitance (F/cm), gate area (cm²), extrinsic Debye length, thermal energy at room temperature (J), electron charge (C) and 90% W_{max} of Na or Nd respectively. After C-V characterization, a set of samples from this run was subjected to the post-metallization annealing at a temperature of 400 °C for 30 min. The C-V of these samples measured between -10 V to +10 V and +10 V to -10 V still show a significant hysteresis of 5 V, as shown in curves 'i' and 'j' of Figure 1. Another set of samples from the same run were subjected to PMA at a temperature of 600 °C for 30 min. The capacitance voltage curves from -10 V to +10 V and from +10 V to -10 V show a significant reduction in the hysteresis by 3 V as shown in the curve 'k' and 'l' of the Figure 1, compared to the as-deposited sample. Consequently a large positive flat band voltage shift towards positive side of gate voltage in the samples was observed after PMA. This shift in the flat band voltage of the as-deposited and PMA treated samples may be attributed to the presence of high density positive defect charges at the nitride/silicon interfaces. As evident from, the hysteresis in C-V curves as shown in Figure 1. The observed hysteresis may be attributed to the hole trapping and de-trapping mechanism of Si/Si₃N₄ interfaces, and not due to dielectric polarization or ionic displacement (e.g. Na⁺, K⁺, etc.) in the nitride dielectric film, which contribute to the effective oxide charge (Q_{EFF}) [3].

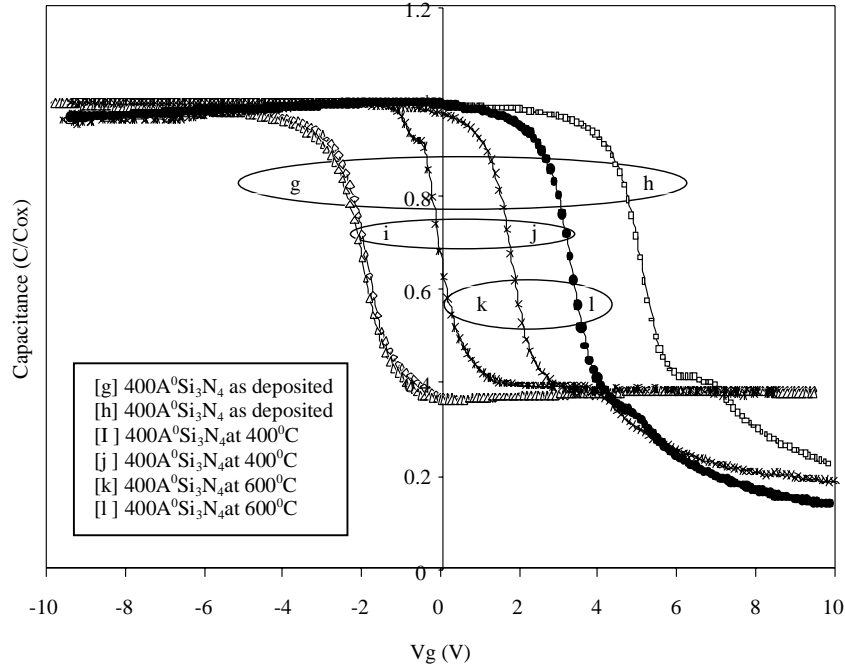


Figure1. C-V (normalized) characteristics of Al/Si₃N₄/Si based as MIS structure, showing hysteresis of as-deposited and after PMA at 400 °C and 600 °C measured at 1 MHz frequency. The curves were obtained by gate voltage sweeping from forward to reverse and back.

The effected oxide charge in the dielectric film is calculated from the relation

$$Q_{EFF} = \frac{C_{ox}(W_{MS} - V_{FB})}{A}, \quad (3)$$

where C_{ox} , W_{MS} , V_{FB} and A are the oxide capacitance, metal-semiconductor work function difference (V), flat-band voltage and gate electrode area (cm²).

In the forward sweep, when the gate bias is varied over -10 V to $+10$ V, the Si interface goes from accumulation to weak inversion [3, 10]. Since the as-deposited Si_3N_4 sample was grown by PECVD, there could be high density of hole-trapping sites at the Si/ Si_3N_4 interface and these trapping sites could be filled with the majority carrier holes [8, 11]. The excess positive charge thus trapped at the interface will give rise to the flat band voltage (V_{FB}) shift in the forward bias (-10 V to $+10$ V) C-V curve. When the gate voltage approaches the weak inversion region, de-trapping of the trapped holes will occur by charge exchange with the Si substrate. Although the structure at the weak inversion does not favor a strong hole de-trapping process, the amount of positive charge de-trapped will be sufficient to cause the positive flat band voltage (V_{FB}) shift observed in the reverse bias ($+10$ V to -10 V) in comparison with the forward bias of cyclic C-V curve [3]. The positive shift of the C-V curves indicate the reduction of positive fixed charges and the hole trapping sites intrinsic to the Si_3N_4 , due to PMA at temperatures of 400 °C and 600 °C and contribute to the reduction in effective oxide charges (Q_{EFF}). The presence of reduced hysteresis in the forward and reverse C-V curve indicates that the oxide hole traps at the Si/ Si_3N_4 interfaces have been reduced after post-metallization annealing [12, 13]. Therefore, it is interesting to point out that the significant variation of the memory window of CV characteristics, due to the flat-band voltage shift. It is observed maximum shift in the as-deposited samples as compared to the PMA treated samples. This implies that PMA in silicon-nitride based system is responsible for tailoring the flat-band voltage shift in the memory devices or, in other words, tailoring the memory window of the non-volatile devices. The electrical parameters computed from CV data are given in Table.

Table. Parameters Obtained from C-V Measurement.

Parameters	As-deposited	After PMA at 400 °C	After PMA at 600 °C	As-deposited	After PMA at 400 °C	After PMA at 600 °C
	Forward Sweep of Si_3N_4			Reversed Sweep of Si_3N_4		
V_{FB} (V)	0.4	0.6	1.8	6.5	4.7	2.3
V_{TH} (V)	0.9	1.2	2.4	7.3	5.4	2.8
$Q_{EFF} \times 10^{-7}$ (C/cm ²)	- 7.3	-5.9	-4.3	-6.9	-5.6	-4.2

Silicon nitride dielectric films were deposited by PECVD technique with the help ammonia (NH_3), silane (SiH_4), nitrogen (N_2) plasma. As a result we have a such type of reactive species and hydrogen containing silicon reactants, ($<5\%$) [11]. Hence following PMA, these hydrogen containing species diffused out, and the strained Si-O and weak Si-H bonds were replaced by strong and rigid Si-N bonds to [10, 14] from nitride films that would result in the improvement of the hysteresis due to low densities of effective oxide charges and moderating the interface traps in the MIS structures.

3.2. Effect of PMA on G-V curve

The conductance technique is considered to be one of most sensitive techniques for the measurement of interface state density. It is assumed that the interface states are in equilibrium with the substrate and that the gate to interface state tunneling time constant is much longer than the interface state time constant for gate dielectric thickness of more than 2 nm [15]. Defects can exchange charge with the silicon. They can interact with the silicon conduction band by capturing or emitting electrons and with valence band by capturing or emitting holes. Capture or emission occurs when interface traps change occupancy. Changes in the occupancy can be produced by changes in the gate bias. In the conduction method, interface trap levels are detected through the loss resulting from changes in their occupancy produced by variations of gate voltage [16]. The measured conductance G_m , the corrected conductance G_c and corrected capacitance C_c

in accumulation across the MIS capacitor are given by the following relations [14]:

$$C_{m,acc} = \frac{C_{ox}}{1 + \omega^2 R_s^2 C_{ox}^2}; \quad (4)$$

hence

$$C_{ox} = C_{m,acc} \left[1 + \left(\frac{G_{m,acc}}{\omega C_{m,acc}} \right)^2 \right]. \quad (5)$$

Therefore corrected capacitance C_c is

$$C_{corrected} = \frac{(G_{m,acc}^2 + \omega^2 C_{m,acc}^2) C_{m,acc}}{a^2 + \omega^2 C_{m,acc}^2}, \quad (6)$$

and corrected conductance G_c is

$$G_{corrected} = \frac{(G_{m,acc}^2 + \omega^2 C_{m,acc}^2) a}{a^2 + \omega^2 C_{m,acc}^2}, \quad (7)$$

respectively, where $a = G_{m,acc} - (G_{m,acc}^2 + \omega^2 C_m^2) R_s$, C_m is the measured capacitance, G_m is the measured conductance, $C_{corrected}$ is corrected capacitance for series resistance and $G_{corrected}$ is the corrected conductance for series resistance; $\omega = 2\pi F$, where $F = 1$ MHz. If conductance G_p is of the order of $1/R_s$ (R_s is series resistance), the term $G_c R_s$ tends to dominate and hence it causes a frequency independent effect [15]. The G-V response measured at 1 MHz is shown in Figure 2. Therefore, it is more important to understand conductance-voltage characteristics for the PECVD based dielectric films, which using traps based memory nodes for write, store and erase programs. Hence the corrected conductance G_c shows a significant hysteresis and is a function of gate bias voltage from -10 V to $+10$ V, (forward sweep) and from the $+10$ V to -10 V (reverse sweep), as shown in Figure 2(g, h). In accumulation, majority carrier density is very large near the Si-Si₃N₄ interface, so the rate of interface traps capture are fast at 1 MHz frequency. Interface traps levels respond immediately to the ac voltage, and no loss occurs. In depletion region, capture rates slow down, and interface trap levels cannot keep in phase with the ac voltage. Hence there is a loss in the majority-charge carriers at the Si-Si₃N₄ interface. There is a presence of hysteresis in the conductance peak (830 μ s and 810 μ s for curves (g) and (h) in Figure 2) at the interfaces of as-deposited samples. The high conductance values indicate the higher densities of interface traps at the Si/Si₃N₄ interface. As we approach towards further in depletion near mid-gap region, majority carrier density becomes so low that the interface trap levels hardly respond. The capture rate is so low that almost no carriers are exchanged between interface trap levels and the silicon. Therefore the loss of the carriers is negligible [14]. After PMA at 400 °C and 600 °C there is a reduction in the conductance peak (750 μ s, 660 μ s and 600 μ s, 550 μ s for the curves (i), (j) and (k), (l) in Figure 2). The reduction in the conductance peak as well as the shift in the width of the (G-V) curve hysteresis towards positive side of the gate voltage after PMA indicated the variation of memory window of MIS devices. Figure 2 curves (i), (j) and (k), (l) indicate that the interface traps at the Si/Si₃N₄ interface have been moderated after PMA as observed by C-V curves in Figure 1.

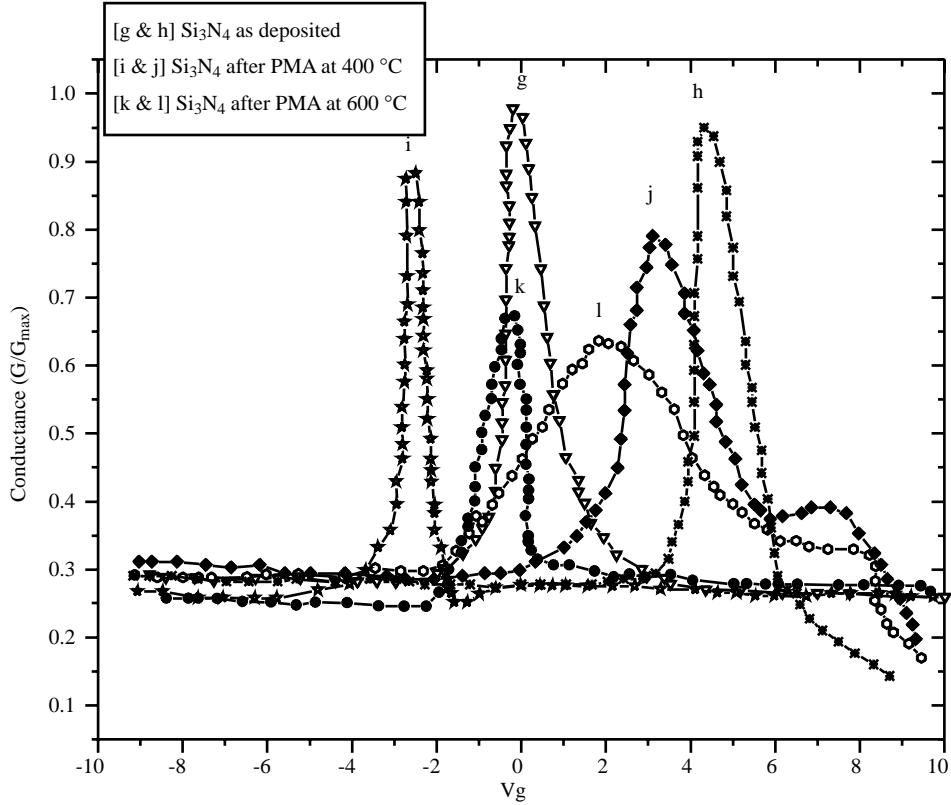


Figure 2. The corrected conductance G_c normalized by the maximum value of the corrected conductance G_{max} of the as-deposited sample during the forward sweep for the different samples measured at 1 MHz frequency.

3.3. Effect of PMA on D_{it} of Si/Si₃N₄ Structure

The interface trap density versus band-gap energy curve examine, the trap densities near the Si₃N₄/Si interface and can highlight any defects formed by PECVD deposition process. The interface trap density of Si₃N₄/Si interface of Figure 3 curve (g) increases more rapidly toward the mid band-gap. Therefore starting from the conduction band edge with higher initial interface traps are in the Si₃N₄/Si interface. It ends up with a higher number density at Si₃N₄/Si interface as the energy approaches to mid-band gap of the Si₃N₄/Si interface. Hence Al/Si₃N₄/Si interface is more diffused interface [6]. After PMA at 400 °C and 600 °C the interface state density D_{it} is significantly reduced in the order of two in case of Si₃N₄/Si (Figure 3, curves (i) and (k)) interface. The increase of trap density in the dielectric is followed by a proportional increase of interface traps and also by an increase of fixed oxide charges. The interface trap density is calculated from the interface state capacitance C_{it} from the relations

$$C_{it} = (1/C_q - 1/C_{ox})^{-1} - (1/C_H - 1/C_{ox})^{-1}, \quad (8)$$

$$D_{it} = C_{it}/A. \quad (9)$$

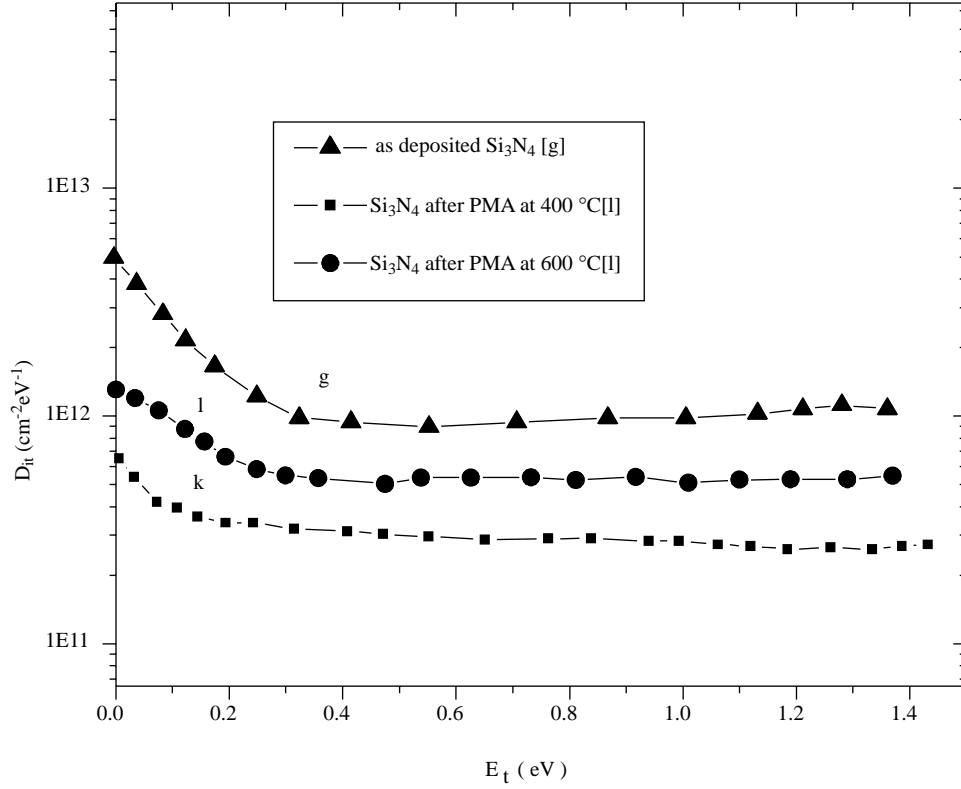


Figure 3. The interface state density D_{it} at Si/Si₃N₄ interface of as-deposited and after PMA at 400 °C and 600 °C for forward sweep.

Here, C_q , C_H , D_{it} and A are quasistatic capacitance, high frequency capacitance, interface state density and electrode area, respectively. This result indicates that there is significant reduction of fixed oxide charges after PMA, as already observed in the previous work using capacitance-voltage (C-V) and conductance-voltage (G-V) measurements [14]. Therefore, it is suggested PMA based modernization of trap-assisted charging/ discharging processes is what generates the long-term retention time.

4. Current Voltage (I-V) Characteristics of Al/Si₃N₄/Si Structures

Due to continuing growth in the integration density of integrated circuits, and reliability problems with SiO₂ as a gate dielectric material hinders future integration technology, there is thus need for higher quality insulators to replace SiO₂ in the scaled down regime. Silicon nitride among other high-K dielectrics is at the forefront of research. Therefore, gate leakage current density J (A/cm²) as a function of electric field E (MV/cm) of as-deposited Al/Si₃N₄/Si structure and following PMA treated samples were investigated, the results shown in the curve of Figure 4. It was observed that the PMA treated samples have lower gate leakage current compared to the as-deposited samples. This reduction in gate leakage current, attributed to the PMA, reduced the localized charges with in the gate nitride films compared to as-deposited samples. Poole-Frenkel (P-F) leakage current from silicon nitride based MIS structure is shown in Figure 5. The dielectric constant ϵ computed from the P-F plot for as-deposited and after PMA treatment at 400 °C and 600 °C were 6.2, 6.4 and 6.7, respectively. That PMA treatment reduced leakage current is attributed to densification of silicon nitride films compared to the as-deposited films [11, 13].

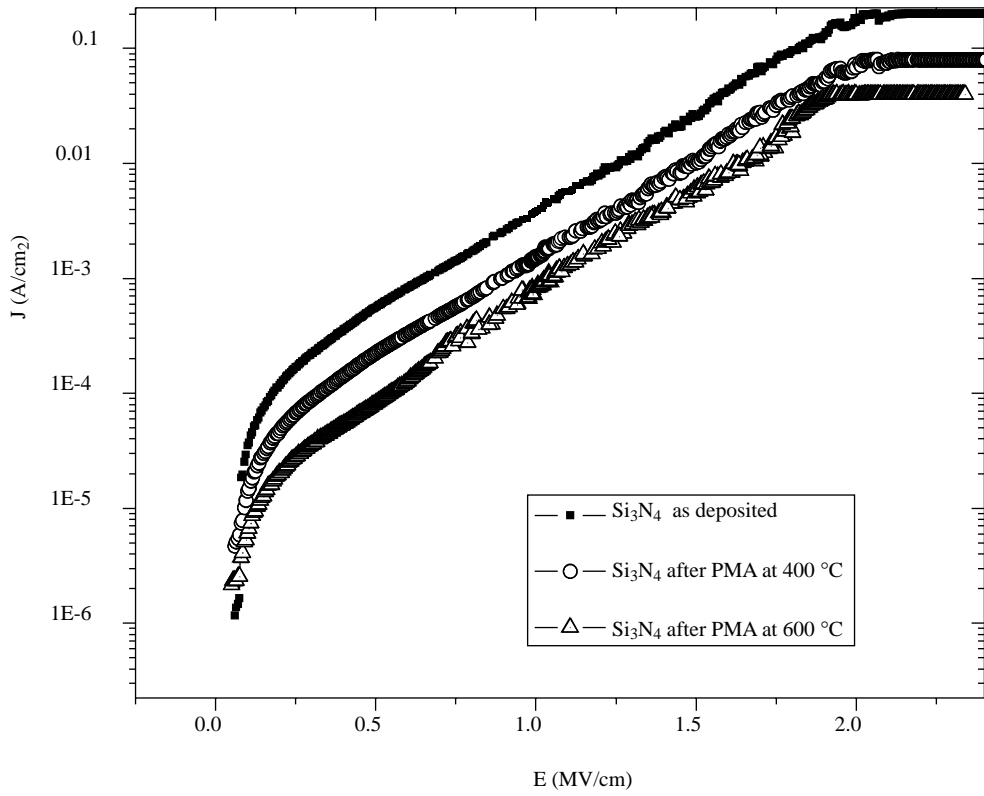


Figure 4. J as a function for E of Al/Si₃N₄/Si structure as-deposited and after PMA at 400 °C and 600 °C.

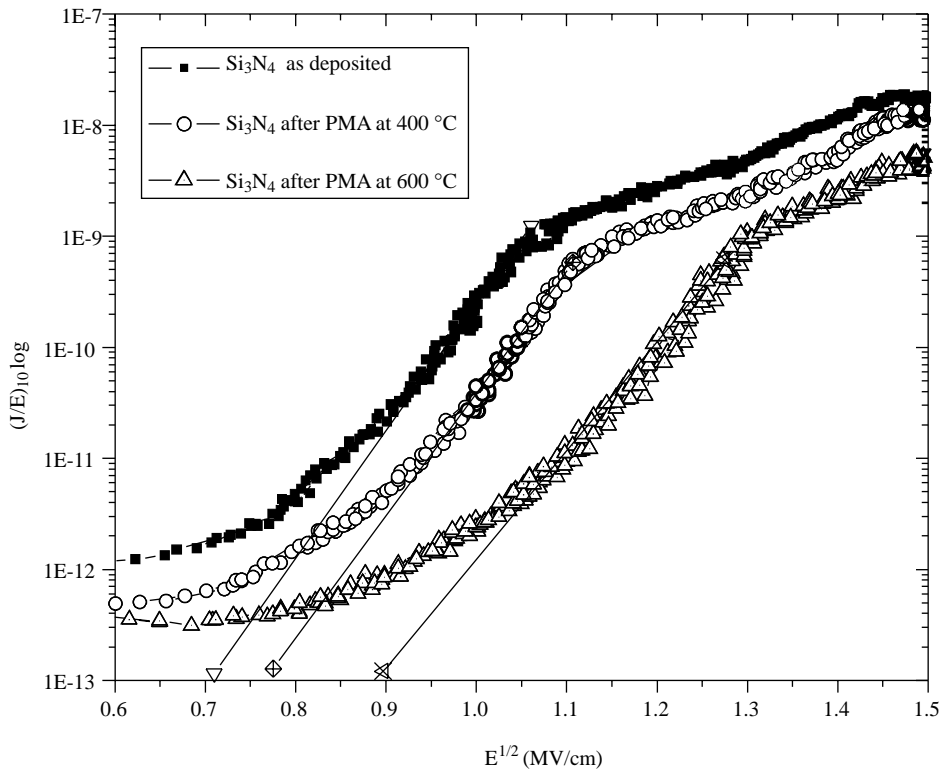


Figure 5. PF tunneling in Al/Si₃N₄/Si Structure.

Fowler-Nordheim (FN) tunneling plot of these samples is shown in Figure 6. The F-N tunneling barrier height of Al/Si₃N₄/Si MIS capacitors was calculated via the F-N plot in Figure 6. It was observed that the effective barrier height of as deposited samples were 2.4 eV and after the Post Metallization Annealing (PMA) treated at 400 °C and 600 °C, the barrier height became 2.6 eV and 2.9 eV, respectively. These results are attributed to the presence of charges in PECVD as-deposited silicon nitride dielectric films, and these charges not only produce the J-E shift, but also vary the effective barrier height. The effective barrier height, however, was changed if the charge centroid was inside the tunneling distance. Specifically, the charges near the Si₃N₄/Si interface gave a flat-band voltage shift and varied the effective barrier height for positive charges [17, 18]. In deduction, the Post Metallization Annealing treatment decreased the fixed positive charges inside this dielectric film, as indicated by the J (A/cm²) and E (MV/cm)⁻¹ curves of PMA treated samples, compared to the as-deposited samples. In addition, increment in the effective barrier height for the PMA-treated sample indicated the presence of positive charges near the interface, and thus is also consistent with the result of high-frequency C-V characteristics shown in Figure 1. PMA caused reduction in localized states and improved the electrical properties of silicon nitride based MIS structure and increase the reliability of the memory window for non volatile devices, which led to increase in stoichiometry of the silicon nitride based dielectric films after PMA treatment; while the as deposited nitride samples exhibits the highest charge storage trapping sites due to larger memory window. The lower leakage current resulting after PMA in the Si₃N₄ indicates PMA as the key parameter moderating the defect density in the Si₃N₄ and generates a long-term retention time capability with in the dielectric film. This also suggested that the probably the positive and negative oxide charges before PMA as shown in Figure 1 and Figure 2 account for relatively high leakage current. This increased leakage current is considered to be due to trapping and de-trapping sites at Si/Si₃N₄ interfaces of the dielectric film.

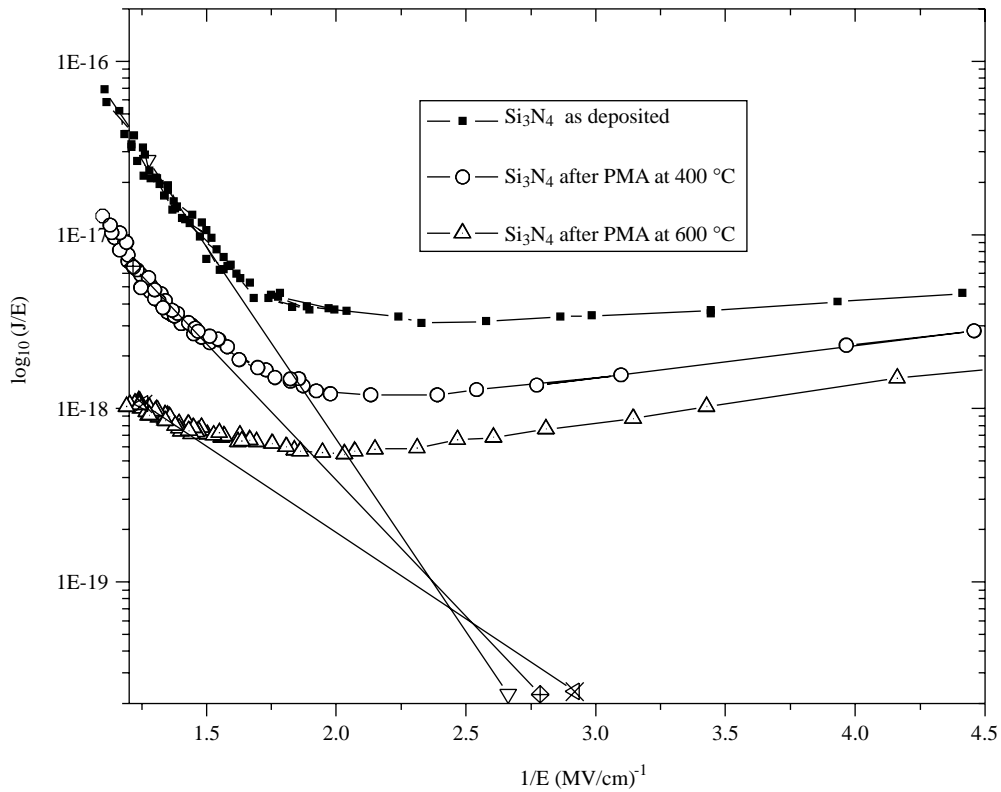


Figure 6. FN tunneling in Al/Si₃N₄/Si structure.

5. Conclusion

The improved memory operations were demonstrated based on the trapping and de-trapping of carrier from memory location at the Si₃N₄/Si interface. The significant shift in flat-band voltage shift V_{FB} in the CV characteristics can be attributed to the stored electrons/holes falling into defect states of silicon-nitride films. The charge-loss rate was approximately similar to SiO₂/Si based memory devices, compared to memory devices, which gave rise to a remarkable increase of the memory retention time. Trap-assisted charging/discharging processes were suggested to generate a long-term retention time of the Si/Si₃N₄/Al based memory cell.

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