Low leakage pocket junction-less DGTFET with biosensing cavity region

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Abstract: Low leakage current junction-less double gate tunnel field-effect transistor (JLDGTFET) with narrow band gap material pocket region of Si0.7Ge0.3 shows increased band to band tunneling and sharp subthreshold characteristics to meet low power, high speed digital and memory applications. The proposed JLDGTFET exploits the junction-less behavior that supports reasonable values of ON/OFF currents as well as improved subthreshold parameters. First, the performance optimization of the JLDGTFET is carried out with different gate contact and oxide region materials in terms of $I_{ON}/I_{OFF}$ current ratio, subthreshold slope, and drain induced barrier lowering. The ON/OFF performance of the pocket Si0.7Ge0.3 JLDGTFET with cavity region is also examined to enhance the sensing capability for biomolecules present in the atmosphere that affect the dielectric constant of air present in the cavity and hence overall performance changes. The 2D/3D Visual TCAD tool is used to simulate novel thin body pocket Si0.7Ge0.3 JLDGTFET.

Key words: Junction-less double gate tunnel field-effect transistor, BTBT tunneling, heterojunction tunnel field-effect transistor, narrow band gap material

1. Introduction

Technology scaling needs minimization of power dissipation, which enhances the battery life of portable devices. Multigate MOSFET structures (double-gate, triple-gate, and gate-all-around MOSFETs) designed over SOI wafers show more control over the gate in the subthreshold region and have low power consumption due to less leakage in comparison to conventional MOSFETs [1, 2]. The thermal limit imposes conditions on further miniaturization of MOSFET structures, causing degradation in subthreshold performance at low drain voltage. A tunneling field-effect transistor (TFET) is less affected by the conditions imposed due to thermal limits and may perform better at low drain voltage. A positive drain bias makes the TFET reverse-biased, with the band to band tunneling current modulated by gate voltage under this condition where charges in the channel come mainly from the drain side rather than the source [3]. Here, band to band tunneling in the TFET follows the charge-plasma concept, depending upon work function of the metallic gate contact in the source/drain region and silicon body thickness less than the Debye length [4]. The Debye length is governed by the following expression:

$$L_D = \sqrt{\frac{V_T \varepsilon_{Si}}{qN}}$$

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where N represents carrier concentration, \( \epsilon_{\text{Si}} \) represents the dielectric constant of silicon, and \( V_T \) is thermal voltage.

Narrow band gap III–V materials have the potential to optimize thin body TFET performance [5, 6] with adequate improvement in tunneling properties. GaSb–EDTFET was presented with enhanced on-state current, transconductance, and cut-off frequency due to high tunneling efficiency and the high-electron mobility of GaSb compared with Si-EDTFET [7]. A quantum model with atomistic simulations was used to characterize the subthreshold performance of GaSb, InAs, and InGaAs TFET (heterojunction TFET) [8–10]. A double-gate TFET device was designed by Rahi et al. with a very good \( I_{\text{ON}}/I_{\text{OFF}} \) ratio (10^{12}) and low SS (41.54 mV/dec) [11]. The tunnel FET emerged as a potential candidate in digital and memory designs in the low power regime below 20 nm technology nodes [12]. A doping-less TFET [13] was designed with an intrinsic channel region, heavily doped drain, and source region. Low doping in the channel region increases carrier mobility, resulting in increased drain current. Inclusion of junction-less source-channel and channel-drain region controls the parasitic resistance and improves ON-state current. Additional narrow band gap material (Ge, SiGe, etc.) pocket regions in heterojunction TFETs decrease tunneling distance and enhance tunneling current in ON-state conditions [14–16]. Si-SiGe heterojunctions are preferred due to better matching characteristics of their lattice structures. A heterogate junction-less transistor with high/low–K dielectric was explored for future low power devices [17]. Use of the high-K gate dielectric improves the internal electric field in H-JLTFET, which results in low OFF-state leakage current suitable for ultra-low power applications [18]. The thin dielectric region incorporated in the middle of the channel reduces the OFF-state current and provides good value of \( I_{\text{ON}}/I_{\text{OFF}} \) ratio up to 10^5 [19]. The major drawback of the TFET is longer channel length, which is required to get the equivalent ON-state current in comparison to MOSFET structures similar in dimensions. To limit the short channel effect (SCE) with smaller dimensions, there is a requirement of steep junctions at the source-channel and channel-drain junctions that controls the effective channel length and parasitic resistances. The multiple-gate junction-less transistors were evaluated to rule out the requirement of steep junctions below 20 nm technology [20]. Inclusion of junction-less behavior in double gate FETs has an advantage of high ON-state current even with smaller dimensions, keeping the subthreshold performance under the limit. The conventional junction-less transistors are heavily doped to obtain good values of ON-state current, but this leads to the high random dopant variability. In this work, the transistor channel is considered either as doping-less or low doping, keeping values of source and drain regions’ doping high to minimize random dopant variability. The junction-less aspect also improves the overall current to support the high speed digital circuit. The junction-less field effect transistor (JLFET) with two isolated gates [21, 22] with high-k dielectric material (20 nm gate length) shows excellent characteristics with high \( I_{\text{ON}}/I_{\text{OFF}} \) ratio (10^8) and a point subthreshold slope of 38mV/decade. Practically, it is difficult to control the isolated gate with different gate bias voltages. The proposed junction-less double gate TFET (JLGDFTFET) with p-type \( \text{Si}_{0.7}\text{Ge}_{0.3} \) pocket region implantation mainly suppresses OFF-state leakage (< 10^{-12} A/\mu m) and provides an additional barrier for the charge carriers by reducing the ambipolar nature of the tunneling current. In addition, the metal gate with higher work function and high-K dielectric material as oxide region further increase the \( I_{\text{ON}}/I_{\text{OFF}} \) current ratio. In this paper, a new JLGDFTFET is proposed with narrow band gap material as the pocket region that provides a barrier due to source/drain/channel depletion and p-type pocket region resulting in suppression of transistor parasitic and subthreshold leakage. Using 2D/3D simulations, it is found that the \( I_{\text{ON}}/I_{\text{OFF}} \) ratio is 10^9 for gate length of 15 nm, which is higher than any other design proposed earlier having similar dimensions. The TFET with short gate structure was modeled
with dielectrically modulated biosensing features [23–26], which is a real-time application of emerging TFETs. A FET biosensor with a vertical gap is sensitive to biological conditions, resulting in the variation in threshold voltage [27, 28]. The dielectric modulated FET (DMFET), modeled as a biosensor, shows a considerable change in output with the variation of dielectric constant in the nanogap region [29]. The sensitivity of such FET-based biosensors depends on cavity dimensions. Therefore, the proposed pocket Si$_{0.7}$Ge$_{0.3}$ JLDGFET is further examined with multiple cavity regions incorporated at the source end. The dielectric constant (K) of these cavity regions depends on atmospheric conditions. The changes occurring in the dielectric constant affect the electrical characteristics of transistors, which can be easily measured. Similar to nanomaterial-based biosensors [30], the JLDGFET is also sensitive to the dielectric permittivity nanogap cavity region. The changes in biomolecules can be observed with the variation in dielectric permittivity of the cavity region. Therefore, the proposed JLDGFET with cavity region is capable of sensing atmospheric changes resulting in the change in drain current and threshold voltage.

![Figure 1](image1.png)  
**Figure 1.** 2D Structure of JLDGFET with SiGe pocket region.

![Figure 2](image2.png)  
**Figure 2.** 3D simulation view of JLDGFET device, material view.

### 2. Device model and structures

The 2D Visual TCAD (Cogenda) has been used to implement the new junction-less double gate TFET (JLDGFET). The source and drain are kept at equal doping levels of $10^{20}$ cm$^{-3}$ with 10 nm dimensions. The channel region is considered as doping-less with dimensions of 20 nm to explore the charge plasma concept, showing less dependency on dopant variations. Figure 1 indicates the new 2D JLDGFET structure with depth gate height $H_g = 4$ nm and length $L_g = 15$ nm. The proposed device has been investigated with different oxide materials under the gate ($SiO_2$, $HfO_2$, etc.) and gate contact materials (Al, Pt, etc.). To increase the band to band tunneling property a pocket region of $Si_{0.7}Ge_{0.3}$ (energy band gap of $< 1$ eV) of 5 nm thickness is included near the source region under the influence of the gate. To achieve high ON-state current, a metal gate with high value of work function, made of Pt (5.7 eV), is used with an oxide region made of high-K dielectric material $HfO_2$ (25) replacing $SiO_2$ (3.9) under the gate and performance comparable with the Al/$SiO_2$ interface. Figure 2 shows the 3-dimensional view of the JLDGFET designed with $Si_{0.7}Ge_{0.3}$ pocket region (doping $10^{20}$ cm$^{-3}$) to suppress the off-state current, resulting in higher $I_{ON}/I_{OFF}$ current ratio. Figure 3 shows the 2D view of the JLDGFET with biosensing cavity region of width of 5 nm and depth of 3 nm under both top and bottom gate contacts.

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3. Results and discussion

The proposed JLDGTFTET is analyzed using the Visual 2D/3D TCAD device simulator. Figure 4 represents the energy band diagram of the JLDGTFTET without cavity region with different gate and drain bias conditions. The distance between conduction band minima and valence band maxima is decreasing with increasing gate bias voltage resulting in the increase in ON-state current. Figure 5 shows the hole density distribution in source, pocket, channel, and drain region with the variation in gate and drain bias voltage. The hole density is negligible in the source, channel, and drain region, showing an almost constant nature. In the SiGe pocket region, the hole density shows sharp changes and its value decreases with increase in gate bias voltage. This indicates that the p-type SiGe pocket region acts as an additional barrier in the OFF-state, resulting in low leakage current. Furthermore, the simulation is performed for the JLDGTFTET ($L_g = 15$ nm) in linear and saturation regions of operation and the performance is compared with a similar junction-based DGTFTET as well as the DGMOSFET.
in terms of ON-state and OFF-state current, subthreshold slope (SS), and DIBL. The proposed JLDGTFTET has very low off-state current due to the barrier provided by the p-type pocket region resulting in $I_{ON}/I_{OFF}$ current ratio up to $10^9$ ($L_g = 15$ nm), which is higher in comparison to the TDJLT [19], varying between $10^2$ and $10^7$ with $L_g$ varying between 10 and 20 nm. The JLDGTFTET performance is also compared with DGTFET and DGMOSFET, having similar dimensions. Figure 6 shows that the JLDGTFTET has sharp drain current variations with respect to gate voltage in the subthreshold region, showing an advantage over DGTFET and DGMOSFET in both linear ($V_{ds} = 0.1$) and saturation ($V_{ds} = 1$ V) regions.

**Figure 7.** $I_d$ vs. $V_{gs}$ of pocket JLDGTFTET with different gate contact/oxide regions.

**Figure 8.** $I_d$ vs. $V_{gs}$ of pocket JLDGTFTET for ($V_{ds} = 0.1$ V & $V_{ds} = 1$ V).

**Figure 9.** $I_d$ vs. $V_{ds}$ of pocket JLDGTFTET for Al/SiO$_2$.

**Figure 10.** $I_d$ vs. $V_{ds}$ of pocket JLDGTFTET for Pt/HfO$_2$.

Figure 7 shows that the JLDGTFTET with Pt/HfO$_2$ as gate/oxide interface has better $I_{ON}/I_{OFF}$ current ratio of $10^9$ in comparison to $10^7$ of the gate/oxide interface made of Al/SiO$_2$. In Figure 8, the proposed JLDGTFTET and all other designs are compared in linear and saturation regions. The JLDGTFTET with
Pt/HfO₂ as gate/oxide interface has the optimum subthreshold performance with a steep subthreshold slope of 148 mV/V (> 60 mV/decade) and DIBL of 5.12 mV/V. The drain current versus drain voltage characteristic of the JLDGTFT with Al/SiO₂ as gate/oxide interface is shown in Figure 9, which matches the ideal behavior of the transistor. A similar drain current versus drain voltage characteristic of the pocket JLDGTFT is also observed in Figure 10 for Pt/HfO₂ as gate/oxide interface. Here the drain current shows a constant nature after a particular value of V_ds for a fixed value of gate voltage and increases with increase in gate voltage (V_{gs}). This indicates that the proposed JLDGTFT has an ideal nature in all cut-off, linear, and saturation regions and therefore can be easily used for analog and digital applications.

Figure 11. Effect of cavity region material on JLDGTFT performance.

Figure 11 shows the application of JLDGTFT with inclusion of cavity region under gate that senses the changes in bio molecule present in atmosphere. A sharp variation is observed in drain current (%15) and threshold voltage with the change in dielectric constant of material present in cavity. This concludes that the proposed device with cavity region is able to sense the minute variations in atmospheric condition.

Table 1. Performance comparison of JLDGTFT with DGTFET and DGMOSFET (L_g = 15 nm).

<table>
<thead>
<tr>
<th>Device type</th>
<th>I_{OFF} [A/µm]</th>
<th>I_{ON} [A/µm]</th>
<th>I_{ON}/I_{OFF}</th>
</tr>
</thead>
<tbody>
<tr>
<td>DGMOSFET</td>
<td>10⁻⁴</td>
<td>10⁻³</td>
<td>10</td>
</tr>
<tr>
<td>DGTFET</td>
<td>1.47 × 10⁻¹⁴</td>
<td>1.13 × 10⁻¹²</td>
<td>76.87</td>
</tr>
<tr>
<td>JLDGTFT with Al/SiO₂</td>
<td>9.11 × 10⁻¹³</td>
<td>1.2 × 10⁻⁵</td>
<td>10⁷</td>
</tr>
<tr>
<td>JLDGTFT with Pt/HfO₂</td>
<td>4.98 × 10⁻¹³</td>
<td>6 × 10⁻⁴</td>
<td>10⁹</td>
</tr>
<tr>
<td>TDJLT [19]</td>
<td>10⁻¹¹</td>
<td>10⁻⁶</td>
<td>10⁵</td>
</tr>
</tbody>
</table>

Table 1 shows that the proposed JLDGTFT has extensive improvement in DIBL (<20 mV/V) and subthreshold slope (>60 mV/V) even with smaller dimensions (L_g < 15 nm). Table 2 shows a comparison of the JLDGTFT for different gate contact materials and oxide under gate in which JLDGTFT with Pt/HfO₂ gives I_{ON}/I_{OFF} current ratio up to 10⁹ in comparison to 10⁷ of the Al/SiO₂ combination and 10⁵ from the available literature [19] with gate length (L_g) of 15 nm. Table 3 shows that the cavity region with nitride has
Table 2. Subthreshold performance comparison of JLDGTFET with other devices.

<table>
<thead>
<tr>
<th>Device type</th>
<th>SS [mV/decade]</th>
<th>DIBL(mV/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DGMOSFET</td>
<td>40.29</td>
<td>5.04</td>
</tr>
<tr>
<td>DGTFTET</td>
<td>20.65</td>
<td>9.11</td>
</tr>
<tr>
<td>JLDGTFET with Al/SiO₂</td>
<td>163.4</td>
<td>13.24</td>
</tr>
<tr>
<td>JLDGTFET with Pt/HfO₂</td>
<td>148.4</td>
<td>5.12</td>
</tr>
</tbody>
</table>

Table 3. Performance comparison of JLDGTFET with or without cavity region.

<table>
<thead>
<tr>
<th>Device type</th>
<th>$I_{OFF}$ [A/µm]</th>
<th>$I_{ON}$ [A/µm]</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$V_{th}$ [V] ($I_d=4 \times 10^{-12}$ [A/µm])</th>
</tr>
</thead>
<tbody>
<tr>
<td>JLDGTFET with cavity air</td>
<td>$2.15 \times 10^{-13}$</td>
<td>$3.76 \times 10^{-10}$</td>
<td>1749</td>
<td>0.65</td>
</tr>
<tr>
<td>JLDGTFET with cavity SiO₂</td>
<td>$2.15 \times 10^{-13}$</td>
<td>$2.15 \times 10^{-8}$</td>
<td>$10^3$</td>
<td>0.45</td>
</tr>
<tr>
<td>JLDGTFET with cavity nitride</td>
<td>$2.15 \times 10^{-13}$</td>
<td>$6.7 \times 10^{-7}$</td>
<td>$3 \times 10^6$</td>
<td>0.35</td>
</tr>
<tr>
<td>JLDGTFET without cavity</td>
<td>$4.98 \times 10^{-13}$</td>
<td>$6 \times 10^{-4}$</td>
<td>$10^9$</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Table 4. Comparison of JLDGTFET with other TFETs for cavity region dielectric constant K = 1 (air as dielectric material).

<table>
<thead>
<tr>
<th>Device type</th>
<th>$L_g$ [nm]</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$V_{th}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[24]</td>
<td>100</td>
<td>$10^4$</td>
<td>1</td>
</tr>
<tr>
<td>[25]</td>
<td>42</td>
<td>$10^3$</td>
<td>0.85</td>
</tr>
<tr>
<td>[26]</td>
<td>53</td>
<td>$10^3$</td>
<td>0.8</td>
</tr>
<tr>
<td>JLDGTFET</td>
<td>15</td>
<td>$10^4$</td>
<td>0.65</td>
</tr>
</tbody>
</table>

higher ON/OFF current ratio with lower threshold voltage in comparison to air and SiO₂ as cavity region material. Table 4 shows a comparison of the JLDGTFET with the state-of-the-art versions.

4. Conclusions

The proposed pocket $Si_{0.7}Ge_{0.3}$ JLDGTFET with Pt/HfO₂ as gate contact and oxide material shows $I_{ON}/I_{OFF}$ current ratio of $10^9$ in comparison to $10^5$ of the SOI-based TFET with thin dielectric region proposed in the existing literature. The high value of $I_{ON}/I_{OFF}$ current ratio, low DIBL ($<20$ mV/V), and steep subthreshold slope ($>60$ mV/V) of the JLDGTFET makes it suitable for low power, high speed applications and further supports the scaling trends below 20 nm technology nodes. Also, the proposed pocket $Si_{0.7}Ge_{0.3}$ JLDGTFET has been explored with cavity region under gate that enhances the biosensing capability of the transistor depending on the atmospheric changes. The cavity region shows a very sharp change (15%) in drain current versus gate voltage characteristics with different dielectric constant materials present in the cavity region in comparison to other mentioned studies in Table 4 even with smaller dimensions ($L_g = 15$ nm). Thus, the proposed design with biosensing cavity is able to sense the difference in biomolecules present in the atmosphere, showing sharp variations in current and threshold voltages.
Acknowledgment

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References


