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A single operational amplifier-based grounded meminductor mutators and their applications

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Abstract: In this work, three simple configurations of meminductor mutator are presented. The first two configurations of meminductor mutator have been implemented utilizing one CMOS-based operational amplifier, one memristor, one capacitor, and five resistors, while the third configuration of meminductor mutator is implemented utilizing one CMOS-based operational amplifier, two memristors, one capacitor, and four resistors. The implementation and simulation of the proposed configurations are done by using LTspice tool. The viability of the proposed circuits is demonstrated by utilizing TSMC 180 *nm* CMOS technology parameters. The proposed circuits of the meminductor have a simple structure in contrast to many of the circuits presented in the literature and operate satisfactorily over a wide range of frequencies. The functionality of the proposed circuits is verified through utilization of both the spice model of memristor and a memristor emulator circuit. A chaotic oscillator and second-order high pass filter are designed using the proposed meminductor to verify its workability.

Key words: Meminductor, pinch hysteresis loop, memristor, emulator, operational amplifier

1. Introduction

In 1971, the fourth missing fundamental component of a circuit called a memristor was theoretically introduced by Prof. Leon Chua [1], following a resistor, an inductor, and a capacitor. HP Labs physically implemented this nanoscale solid-state device in 2008 [2], which sparked a great deal of attention among researchers. This memristive device has nonvolatility, nonlinearity, and nanoscale size properties. Further, nanoscale memristors have fabrication compatibility with the CMOS process. The first functional memristor array constructed on a CMOS chip was announced by HRL Laboratories [3]. KNOWM company has commercialized the memristors but they have strict operational conditions [4]. Henceforth, researchers engage in the development of diverse memristor models and emulators for the purpose of analyzing and implementing a spectrum of real-world applications [5–8]. The memristor was expanded in 2009 to include a meminductor and a memcapacitor, whose characteristics are dependent on the device's history [9]. These three memory components share traits like nonvolatility and pinched hysteresis loops between the two quantities that characterize them. These mem-elements i.e. memristor, meminductor, and memcapacitor opened a new era of analog memory components for a variety of applications, including adaptive filters [10], chaotic oscillators [11], neuromorphic circuits [12], digital low-

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power computation [13], and many more. Researchers have offered numerous SPICE models of meminductors in the literature [14, 15]. Since a meminductor is not available as a commercial device, numerous circuits of meminductor emulators are reported in research publications to physically examine the dynamics of meminductive devices in the electronic domain. The published work describes a variety of meminductor emulators that were implemented using active and passive elements. In order to convert a memristor into a memcapacitor and a meminductor, D. Biolek et al. presented a synthesis of mutators [16]. In Ref. [17], Pershin and Di Ventra introduced a circuit that transforms the memristor into a meminductor and memcapacitor. But these mutations were not precise, and approximately analogous circuits contained parasitic resistances. After a few years, Pershin and Di Ventra proposed the current conveyor-based emulator to convert memristor into meminductor and memcapacitor, which do not have any additional resistance [18]. In Ref.[19], a meminductor emulator circuit implemented by using a mutator was presented by Sah et al. However, the presented meminductor employs a large count of active and passive elements and has a very low-frequency range. A meminductor emulator based on a memristor-less charge-controlled technique was presented by Sah et al. [20], which is complex in structure because it requires an analog multiplier, operational amplifiers, and several MOSFETs for its implementation. M. E. Fouda et al. presented voltage and current-controlled meminductor emulators which were realized using two mathematical models [21]. A 4-port mutator was introduced by S. Minaei et al. [22], which they used to implement the memristor, meminductor, and memcapacitor. In Ref. [23], operational amplifier-based meminductor emulators are presented and their functionality is verified by realizing a chaotic oscillator. Y. Babacan in his research letter proposed an operational transconductance amplifier(OTA) based meminductor and memcapacitor emulator where there is no requirement for a mutator to perform transformation from memristor to meminductor and memcapacitor [24]. In Ref. [25], a floating/grounded meminductor is implemented using an operational amplifier, operational transconductance amplifier, current conveyors, and passive elements which makes the structure of the circuit complex and bulky. In Ref. [26], a gyrator circuit was used to realize a meminductor emulator. Q. Zhao et al. [27] described a universal emulator to realize meminductor, memcapacitor, and memristor. A meminductor emulator using one analog multiplier, two OTA, and four passive components has been presented in [28]. A meminductor emulator was implemented utilizing the Riordan gyrator in [29]. M.O. Korkmaz et al. realized a meminductor using one analog multiplier, one dual output second-generation current conveyor(DO-CCII), one CCII, and five passive elements [30]. A Colpitts sinusoidal oscillator based on a meminductor emulator was implemented and discussed in detail [31]. In Ref. [32], an operational amplifier-based meminductor emulator is reported and it requires sixteen passive components for its implementation. Meminductor emulator presented in [33] consists of one OTA, one MO-OTA, one voltage multiplier, and three passive elements. The comprehensive analysis details meminductor emulators realized utilizing OTA, CCII, current differencing buffered amplifier(CDBA), and passive components [34–38]. The topology of meminductor reported in [39] is implemented using one voltage differential transconductance amplifier (VDTA) and one DO-CCII whereas the meminductor circuit reported in [40] requires one modified VDTA for its realization. The grounded emulator configuration using two CDBA is reported in [41] which requires fifty CMOS transistors for its implementation. A meminductor emulator based on five CCII and four passive elements is presented in [42]. Meminductor emulators implemented using CDBA, OTA, VDTA, and current differential transconductance amplifier (CDTA) are reported in [43, 44]. Meminductors based on operational amplifiers are reported in [45, 46]. The meminductor presented in [45] functions at a high supply voltage, while the meminductor reported in [46] exhibits a low operating frequency.

Recent literature has revealed that some of the meminductor emulators have complex circuitry since they were designed using analog multipliers and/or a huge count of active blocks and passive components [19–21, 25, 27, 28, 30–33]. Recent research mentions certain emulators that incorporate an excessive number of active devices, leading to complicated designs [32, 34, 35, 37]. The purpose of this work is to construct a meminductor that employs the fewest possible active and passive components.

This work proposes a simple design for a mutator-based meminductor that emulates the behavior of the meminductive system and is realized using a single active block namely an operational amplifier. To implement the proposed designs, CMOS-based operational amplifier, resistors, memristors, and capacitors are used. The fabrication compatibility of CMOS and memristor allows the nanoscale memristor to be fabricated on the top of CMOS layer and therefore memristor does not occupy any implementation area on the chip. The viability of the proposed circuits is demonstrated using both the spice model of a memristor and a memristor emulator circuit.

The organization of the manuscript is as follows: A mathematical review of the memristive, memcapacitive, and meminductive system is provided in Section 2. The design of the proposed meminductors is discussed and presented in Section 3. The analysis and simulation results are summarized in Section 4. In Section 5, a comparison of the proposed and existing models of meminductor is given. In Section 6, a chaotic oscillator and a high pass filter are realized as an application part. Section 7 includes the experimental result of the proposed circuit. Section 8 concludes this work.

2. Review of mem-elements

After building several intriguing memristor-based applications, Di Ventra, Y.V Pershin, and L. O Chua expanded the idea of memory-based circuit elements to inductive and capacitive systems and introduced meminductor and memcapacitor as mem-elements [9]. The electrical relationships that exist between these mem-elements are shown in Figure 1. These mem-element based computers have the capacity to simultaneously store and process information [47, 48]. Memcapacitors and meminductors do not yet have solid-state implementations, which makes it difficult to use their distinctive qualities in real-world applications. Due to this, a new field of study has recently emerged that focuses on developing electronic circuits that fulfill the fundamental equations of the emulated memory elements, or "emulators" of these devices.

In order to demonstrate that the device is a mem-element, the pinched hysteresis curves are produced amid four physical parameters, namely flux (ϕ), charge (q), current (i), and voltage (v) [9]. A charge-controlled memristor is characterized by a correlation between flux, ϕ, and charge, q. Equation (1) is used to define the memristance of a memristor.

$$M_R(q) = \frac{d\phi}{dq} \tag{1}$$

Rewriting (1) as follows:

$$M_R(q) = \frac{\frac{d\phi}{dt}}{\frac{dq}{dt}} = \frac{V(t)}{I(t)} \tag{2}$$

For memristor, a pinch hysteresis curve is drawn either between voltage(v) and current(i) or between flux (ϕ) and charge (q).

A memcapacitor is characterized by a correlation between flux, ϕ, and σ as given in (3).

$$M(c) = \frac{d\sigma}{d\phi} \tag{3}$$

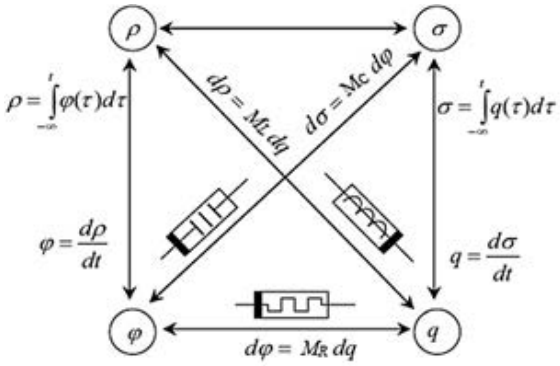


Figure 1. Pictorial representation of interrelation between mem-elements.

where flux (ϕ) is the time integral of voltage and σ is the time integral of charge (q) as shown in (4) and (5):

$$\phi(t) = \int_{-\infty}^{t} V(t)dt \tag{4}$$

$$\sigma(t) = \int_{-\infty}^{t} q(t)dt \tag{5}$$

For memcapacitor, a pinch hysteresis curve is obtained between voltage (v) and charge(q).
A meminductor is defined by a correlation between charge, q, and ρ as given in (6).

$$M_L = \frac{d\rho}{dq} \tag{6}$$

In an alternative form, (6) can be written as

$$M_L = \frac{\frac{d\rho}{dt}}{\frac{dq}{dt}} = \frac{\phi(t)}{I(t)} \tag{7}$$

where q is the time integral of current and ρ is the time integral of flux (ϕ) as shown in (8) and (9)

$$q(t) = \int_{-\infty}^{t} I(t)dt \tag{8}$$

$$\rho(t) = \int_{-\infty}^{t} \phi(t)dt \tag{9}$$

For meminductor, a pinch hysteresis curve is produced amid flux (ϕ) and current (I).

By analyzing various constitutive relationships, it is simple to understand how these variables are interdependent, and by meticulously analyzing the relationship between these variables, memristive systems can be converted into meminductive systems. As a result, the unique property of the memristor, i.e. memory retention can also be achieved in the inductive system. Depending on the input variable, a meminductor can be either defined as a flux-controlled meminductor or a current-controlled meminductor. Equation (10) defines the flux-controlled meminductor, whereas (11) defines the current-controlled meminductor.

$$I(t) = M_L^{-1}(x, I, t).\phi(t) \tag{10}$$

$$\phi(t) = M_L(x, I, t).I(t) \tag{11}$$

where x is the meminductive system's internal state variable, M_L is its meminductance, M_L^{-1} is the inverse of meminductance, and I(t) is the current that is flowing through it.

3. Proposed circuits of meminductor mutator

This part outlines a methodical process for realizing the circuits of a grounded meminductor. The approach involves incorporating memristors into the circuits in a way that allows them to inherit memory retention property, which results in meminductive behavior. As a part of this approach, three different mutator-based circuits have been presented through analytical design techniques. To verify the circuit behavior as a meminductor, the input impedances are calculated for the proposed meminductor circuits. The circuit diagrams are depicted in Figures 2a, 2b, and 2c for the proposed meminductors. In these diagrams, V_i denotes the voltage applied at the input, V_x, the operational amplifier's inverting and noninverting terminal voltages, and V_o, the operational amplifier's output voltage. To implement the proposed circuits illustrated in Figures 2a and 2b, one CMOS-based operational amplifier, one memristor, one capacitor, and five resistors are used, while one CMOS-based operational amplifier, two memristors, one capacitor, and four resistors are used to implement the circuit depicted in Figure 2c.

Applying KCL in the circuit of Figure 2a yields the following set of equations:

$$I_i(s) = \frac{(V_i - V_x)}{R_1} + (V_i - V_2)sC \tag{12}$$

$$\frac{(V_i - V_x)}{R_1} + \frac{(V_0 - V_x)}{R_6} - \frac{V_x}{R_2} = 0 \tag{13}$$

$$\frac{(V_2 - V_x)}{R_3} + \frac{(V_0 - V_x)}{R_5} = 0 \tag{14}$$

$$\frac{(V_x - V_2)}{R_3} + (V_i - V_2)sC - \frac{V_2}{M_{R4}} = 0 \tag{15}$$

The input impedance is found by solving the above set of equations and given in (16):

$$Z_{in}(s) = \frac{V_i}{I_i(s)} = \frac{(\frac{R_1R_5}{M_{R4}R_6} - (1 + \frac{R_1}{R_2})(1 + \frac{R_3}{M_{R4}})) + sC(\frac{R_1R_5}{R_6} - R_3(1 + \frac{R_1}{R_2}))}{(\frac{R_5}{M_{R4}R_6} - \frac{1}{R_2}(1 + \frac{R_3}{M_{R4}})) + sC(\frac{R_1R_5}{M_{R4}R_6} - (1 + \frac{R_1}{R_2})(1 + \frac{R_3}{M_{R4}}) + 1 - \frac{R_3}{R_2})} \tag{16}$$

The input impedance of the circuit becomes meminductive when two matched conditions are applied, and these are:

$$(a)R_2 = R_3 \qquad (b)(1 + \tfrac{R_1}{R_2})(1 + \tfrac{R_3}{M_{R4}}) = \tfrac{R_1R_5}{M_{R4}R_6}$$

After substituting the matched conditions in (16), the input impedance can be written as:

$$Z_{in}(s) = \frac{(\frac{R_1R_5}{M_{R4}R_6} - \frac{R_1R_5}{M_{R4}R_6}) + sC(\frac{R_1R_5}{R_6} - R_3(\frac{R_1R_5}{(1+\frac{R_3}{M_{R4}})M_{R4}R_6}))}{(\frac{R_5}{M_{R4}R_6} - \frac{1}{R_2}(\frac{R_1R_5}{(1+\frac{R_1}{R_2})M_{R4}R_6})) + sC(\frac{R_1R_5}{M_{R4}R_6} - \frac{R_1R_5}{M_{R4}R_6} + 1 - \frac{R_3}{R_3})} \tag{17}$$

$$Z_{in}(s) = \frac{sC(\frac{R_1R_5M_{R4} + R_1R_3M_{R4} - R_1R_3M_{R4}}{M_{R4}R_6(1+\frac{R_3}{M_{R4}})})}{(\frac{R_2R_5 + R_1R_5 - R_1R_5}{R_2M_{R4}R_6(1+\frac{R_1}{R_2})})} \tag{18}$$

$$Z_{in}(s) = sCR_1M_{R4}\frac{(1+\frac{R_1}{R_2})}{(1+\frac{R_3}{M_{R4}})} \tag{19}$$

$$Z_{in}(s) = \frac{V_i}{I_i(s)} = sM_L \tag{20}$$

where $M_L = CR_1M_{R4}\frac{(1+\frac{R_1}{R_2})}{(1+\frac{R_3}{M_{R4}})}$ represents the meminductance of the meminductor circuit. The flux stored in the proposed meminductor is calculated by substituting the value of V_i in (4) and given as:

$$\phi(t) = sM_L\int I_i(s)dt \tag{21}$$

Similarly, the input impedance for Figure 2b and Figure 2c can be calculated and given in (22) and (23) respectively.

$$Z_{in}(s) = sCM_{R1}R_4\frac{(1+\frac{M_{R1}}{R_2})}{(1+\frac{R_3}{R_4})} \tag{22}$$

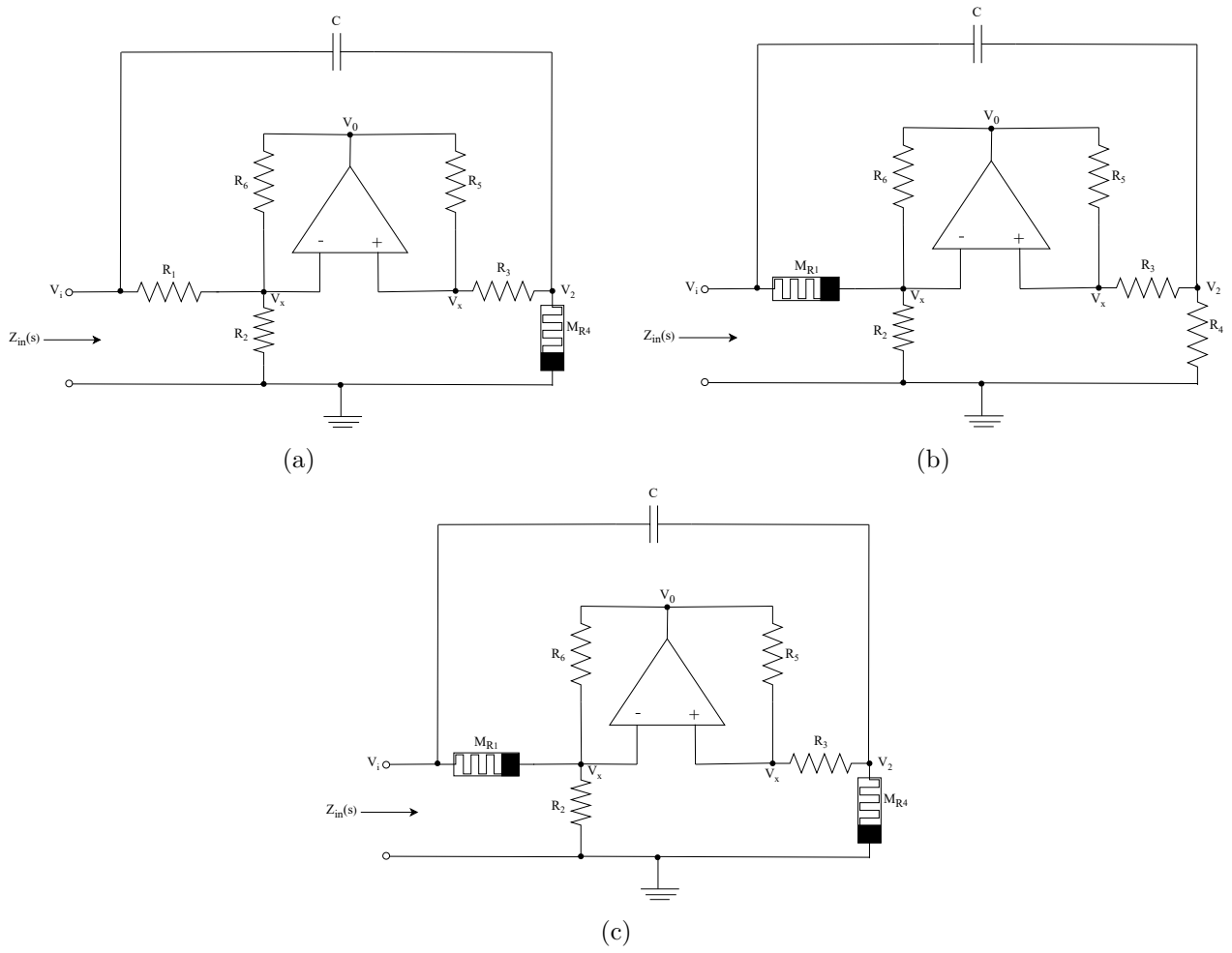


Figure 2. Proposed meminductor mutator circuits.

$$Z_{in}(s) = sCM_{R1}M_{R4}\frac{(1+\frac{M_{R1}}{R_2})}{(1+\frac{R_3}{M_{R4}})} \tag{23}$$

From the above analysis, it is evident that the meminductance of the proposed circuits depends on the value of the memristor, resistor, and capacitor. Since memristors are frequency-dependent, hence meminductance is also impacted by the operating frequency of the circuit.

3.1. Nonideal analysis

The nonideal operational amplifier shown in Figure 3a exhibits parasitic capacitance, C_{ip}, at the inverting and noninverting terminals. At the output terminal, it has parasitic capacitance C_{op} and parasitic resistance R_{op}. The gain of a nonideal operational amplifier is frequency-dependent and can be described using a single-pole model as follows

$$\beta(s) = \frac{\beta_0}{1+\frac{s}{\omega_p}} \tag{24}$$

where β_0 is the open loop dc gain of the operational amplifier at low frequency and ω_p is the pole frequency. The equivalent circuit of the proposed meminductor depicted in Figure 2a considering the nonideal effects is shown in Figure 3b. The analysis of the nonideal circuit depicted in Figure 3b yields the input impedance as

$$Z_{in}(s) = \frac{V_i}{I_i(s)} = \frac{\beta(s)Z_{11} + Z_{12} + sC(\beta(s)Z_{13} + Z_{14}) + sC_{ip}(\beta(s)Z_{15} + Z_{16}) + Z_{17}}{\beta(s)Z_{21} + Z_{22} + sC(\beta(s)Z_{23} + Z_{24}) + sC_{ip}(\beta(s)Z_{25} + Z_{26}) + Z_{27}} \tag{25}$$

where $Z_{11} = \frac{R_1R_5}{M_{R4}R_6} - \left(1+\frac{R_1}{R_2}\right)\left(1+\frac{R_3}{M_{R4}}\right)$, $Z_{12} = \left(1+R_1\left(\frac{1}{R_2}+\frac{1}{R_6}\right)\right)\left(1+(R_3+R_5)\frac{1}{M_{R4}}\right)$

$Z_{13} = \frac{R_1R_5}{R_6} - \left(1+\frac{R_1}{R_2}\right)R_3$, $Z_{14} = (1+R_1\left(\frac{1}{R_2}+\frac{1}{R_6}\right))(R_3+R_5)$

$Z_{15} = \frac{R_1R_5}{R_6} - R_1 - \frac{R_1R_3}{M_{R4}}$, $Z_{16} = (R_1+R_5)(1+\frac{R_3}{M_{R4}}) + R_1R_5(\frac{1}{M_{R4}}+\frac{1}{R_2}+\frac{1}{R_6})$

$Z_{21} = \frac{R_5}{M_{R4}R_6} - \frac{1+\frac{R_3}{M_{R4}}}{R_2}$, $Z_{22} = \left(\frac{1}{R_2}+\frac{1}{R_6}\right)\left(1+(R_3+R_5)\frac{1}{M_{R4}}\right)$

$Z_{23} = Z_{11} + 1 - \frac{R3}{R2}$, $Z_{24} = Z_{12} + \left(\frac{1}{R_2}+\frac{1}{R_6}\right)(R_3+R_5)$

$Z_{25} = \frac{R_5}{R_6} + \frac{R_3R_5}{M_{R4}R_6} - 1 - \frac{R_3}{M_{R4}}$, $Z_{26} = (1+\frac{R_5}{R_6})(1+\frac{R_3}{M_{R4}}) + R_5(\frac{1}{R_2}+\frac{1}{M_{R4}})$

Substituting the value from (24) into (25) and omitting the higher order terms Z_{17} and Z_{27} due to their negligible impact on the overall behavior, simplifies (25) as follows

$$Z_{in}(s) = \frac{V_i}{I_i(s)} = \frac{\beta_0 Z_{11} + Z_{12}(1+s/wp) + sC(\beta_0 Z_{13} + Z_{14}(1+s/wp)) + sC_{ip}(\beta_0 Z_{15} + Z_{16}(1+s/wp))}{\beta_0 Z_{21} + Z_{22}(1+s/wp) + sC(\beta_0 Z_{23} + Z_{24}(1+s/wp)) + sC_{ip}(\beta_0 Z_{25} + Z_{26}(1+s/wp))} \tag{26}$$

Since $\beta_0 >> 1$, it is reasonable to neglect the terms that do not contain β_0. Then, (26) simplifies to

$$Z_{in}(s) \approx \frac{\beta_0 Z_{11} + sC\beta_0 Z_{13} + sC_{ip}\beta_0 Z_{15}}{\beta_0 Z_{21} + sC\beta_0 Z_{23} + sC_{ip}\beta_0 Z_{25}} \tag{27}$$

By putting the values of $Z_{11}, Z_{13}, Z_{15}, Z_{21}, Z_{23}$, and Z_{25} into (27) and further simplifying, we obtain

$$Z_{in}(s) \approx \frac{\frac{R_1R_5}{M_{R4}R_6} - \left(1+\frac{R_1}{R_2}\right)\left(1+\frac{R_3}{M_{R4}}\right) + s\frac{R_1R_5}{R_6}(C+C_{ip}) - s(C\left(1+\frac{R_1}{R_2}\right)R_3 + C_{ip}\left(1+\frac{R_3}{M_{R4}}\right)R_1)}{\frac{R_5}{M_{R4}R_6(1+\frac{R_1}{R_2})} + sC(\frac{R_1R_5}{M_{R4}R_6} + 1 - \frac{R_3}{R_2}) - s\left(1+\frac{R_3}{M_{R4}}\right)\left(C\left(1+\frac{R_1}{R_2}\right) + C_{ip}\left(1-\frac{R_5}{R_6}\right)\right)} \tag{28}$$

In Equation (28), parasitic capacitance C_{ip} is significantly smaller than C. Therefore terms involving C_{ip} pose a negligible impact and can be neglected in comparison to terms involving C. Hence, with this consideration and by applying matching conditions, (28) can be expressed as

$$Z_{in}(s) = sCR_1M_{R4}\frac{\left(1+\frac{R_1}{R_2}\right)}{\left(1+\frac{R_3}{M_{R4}}\right)} \tag{29}$$

The meminductance offered by (29) is analogous to (19), representing an ideal operational amplifier case. Hence, the performance of the proposed meminductor with nonideal effects is found to be satisfactory.

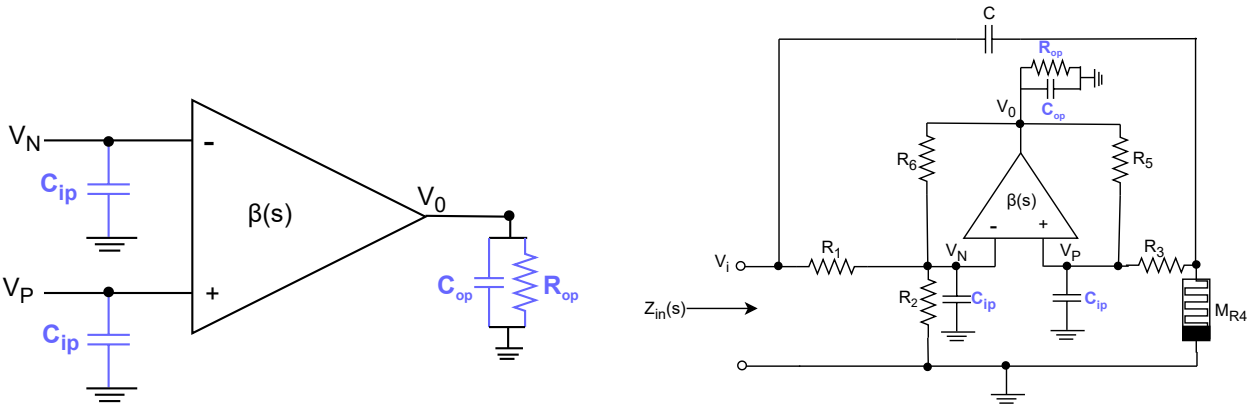


Figure 3. (a) Nonideal operational amplifier and (b) Nonideal equivalent model of proposed meminductor of Figure 2a.

4. Simulation results

To perform simulation of the proposed designs, LTspice Tool is utilized. Simulations have been carried out using the SPICE model of the memristor and CMOS-based operational amplifier. The proposed circuits are also simulated using a memristor emulator circuit. Figure 4 depicts the diagram of a CMOS-based operational amplifier used for the simulation of meminductor. The CMOS-based operational amplifier is implemented using TSMC 180 nm process technology parameters, and Table 1 illustrates the aspect ratio of transistors used for simulation. The CMOS-based operational amplifier's power supply voltage is set as ±0.9 V and the bias current 25 µA. The passive component values utilized for performing the SPICE simulation of the meminductor circuit illustrated in Figure 2a are $R_1 = R_2 = R_3 = 20\ k, R_5 = 6\ k, R_6 = 1.5\ k$, and capacitance of 32 pF. The passive component values for Figure 2b are $R_2 = R_3 = R_4 = 20\ k, R_5 = 6\ k, R_6 = 1.5\ k$, and capacitance of 20 pF. The passive component values for Figure 2c are set as $R_2 = R_3 = 20\ k, R_5 = 3\ k, R_6 = 1.5\ k$, and capacitance of

12 pF. The SPICE model of memristor presented by Z. Biolek et al. [49] and memristor emulator [7] depicted in Figure 5 are used to perform simulations of the proposed circuits. The values of the capacitor are set as 5 pF, 2 pF, and 4 pF to simulate the proposed circuits depicted in Figures 2a, 2b, and 2c respectively, using memristor emulator.

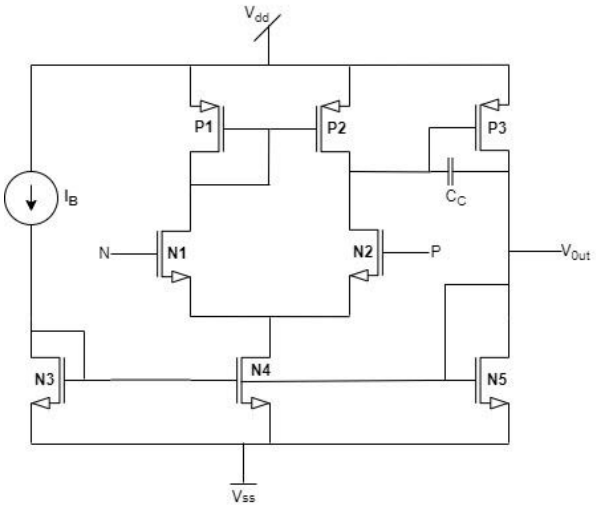


Figure 4. Schematic of the CMOS-based Operational Amplifier.

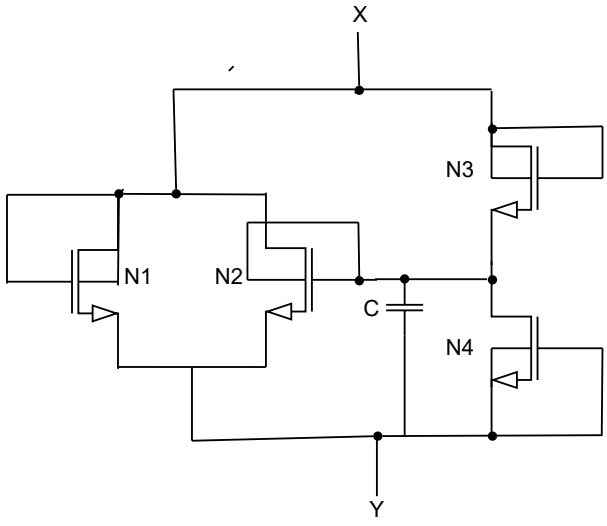


Figure 5. Circuit diagram of memristor emulator [7].

Figures 6, 7, and 8 displayed the simulation results of proposed circuits for transient analysis and associated pinched hysteresis curves at various frequencies using the SPICE model of memristor. Figure 9 illustrates the pinched hysteresis curves of the proposed meminductor circuits at different frequencies, achieved through the implementation of memristor emulator circuit. The pinch hysteresis curve is the key fingerprint of a meminductor circuit to demonstrate its meminductive behavior and for the proposed meminductor the pinch

hysteresis curve is drawn between input flux and current. The time-domain response of the input voltage and current for the proposed circuit of Figure 2a is shown in Figure 10a. In this plot, the input voltage leads to the input current, which confirms the inductive property of the proposed meminductor. The proposed design of Figure 2a is applied with an input pulse (V_i) that has 100 mV amplitude and 1 kHz frequency to test its nonvolatility property. The ratio of flux to current is used to compute meminductance. Figure 10b displays the simulated waveform for meminductance (M_L) and the input pulse(V_i). The waveform in Figure 10b shows that during the on phase of the input pulse, meminductance value increases linearly up to a certain value till the end of the on phase of the input pulse. At the end of the on phase of the input pulse, this value is recorded and retained throughout the off phase of the input pulse. The value of meminductance begins to rise again when the next input pulse's on phase begins, building on the value that was held throughout the preceding input pulse's off time. This demonstrates the proposed meminductor circuit memory retaining property.

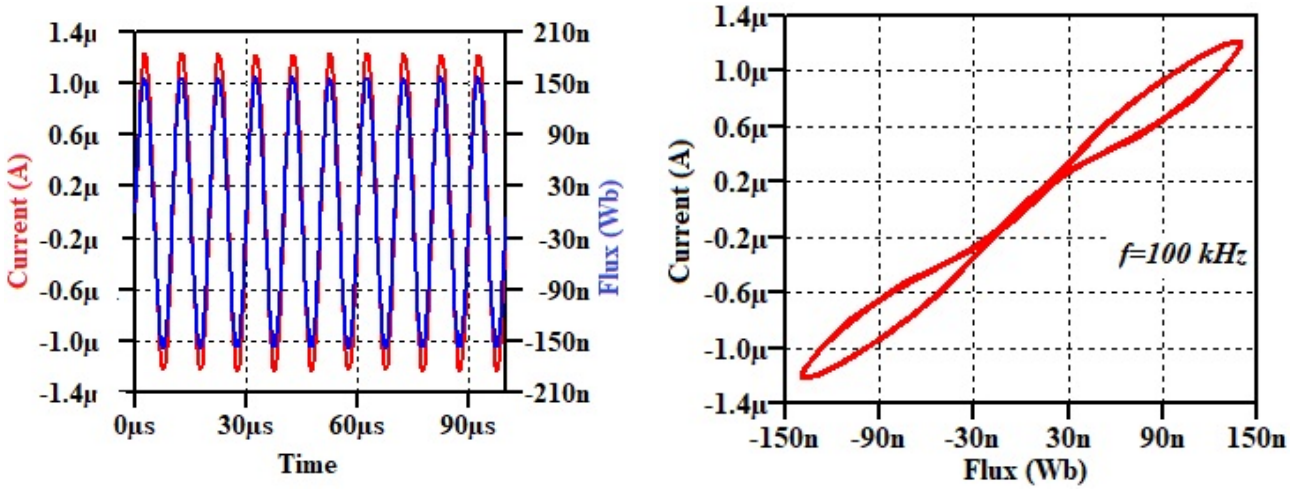
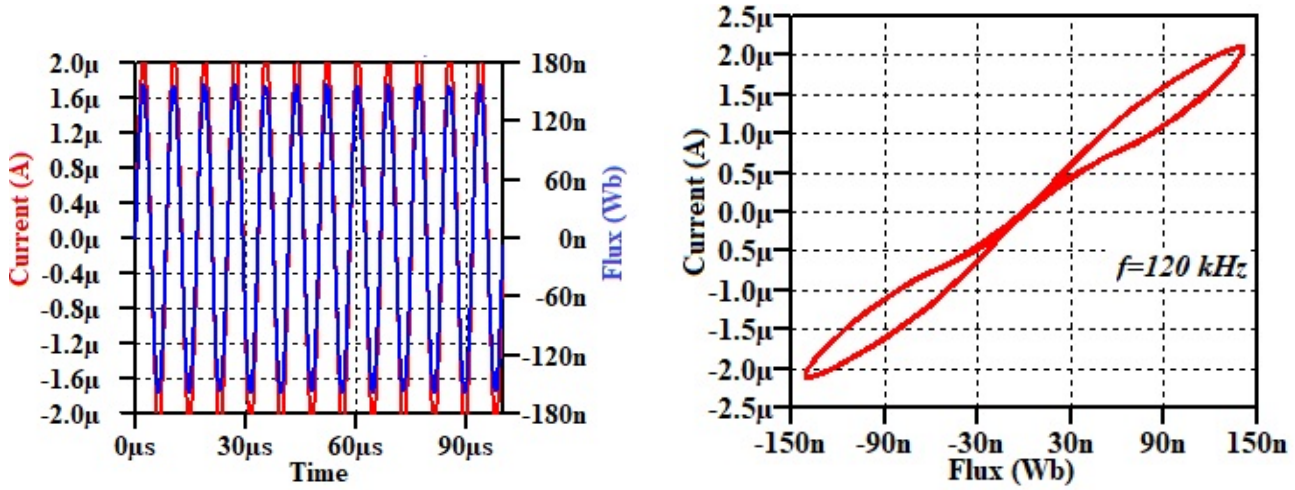


Figure 6. (a) Transient analysis and (b) Corresponding pinch hysteresis loop for the circuit of Figure 2a.

The Monte Carlo simulation has been carried out for two hundred runs to validate the robustness of the proposed meminductor circuits. Figures 11a, 11b, and 11c display the pinch hysteresis loop obtained using Monte Carlo simulation for the proposed circuits of Figures 2a, 2b, and 2c respectively, which verify the resilience of the proposed circuits.

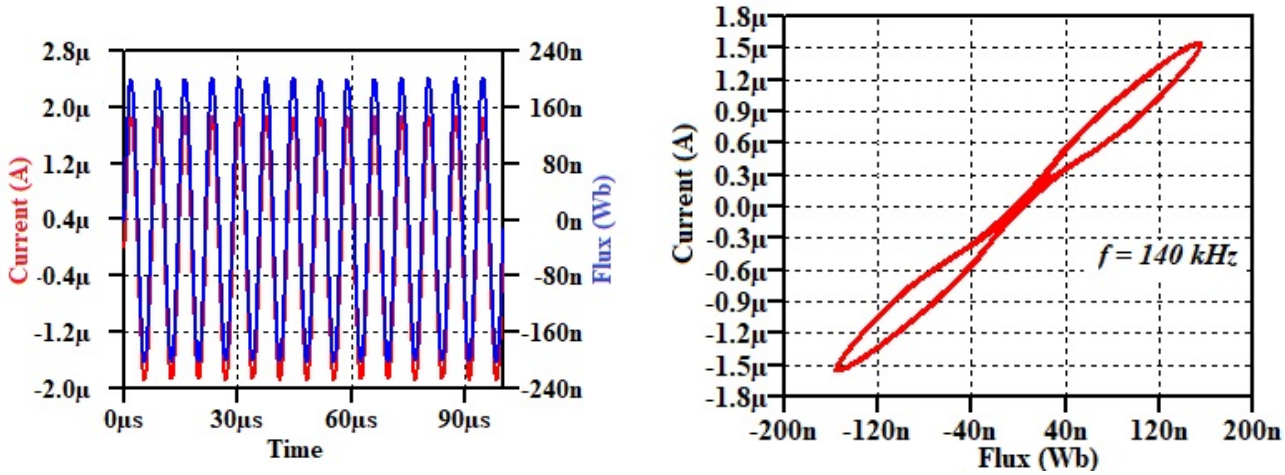
Table 1. Transistors aspect ratio for the CMOS-based operational amplifier.

Transistor	W/L (µm)
P1, P2	6.5/1
N1, N2	28/1
N3, N4	4/1
N5	31.14/1
P3	124.56/1



(a) (b)

Figure 7. (a) Transient analysis and (b) Corresponding pinch hysteresis loop for the circuit of Figure 2b.

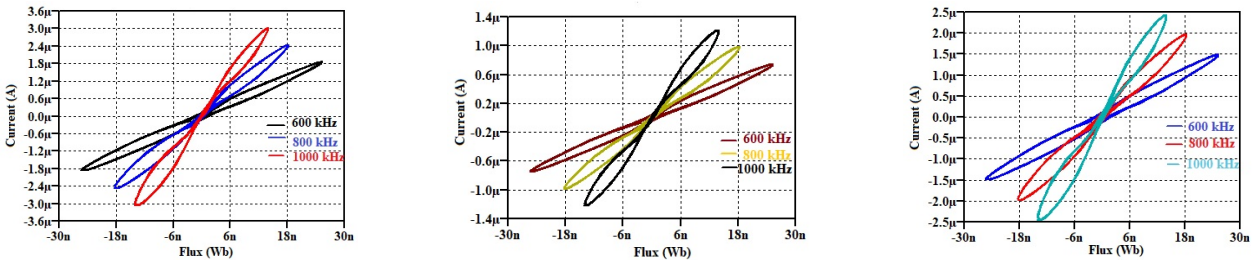


(a) (b)

Figure 8. (a) Transient analysis and (b) Corresponding pinch hysteresis loop for the circuit of Figure 2c.

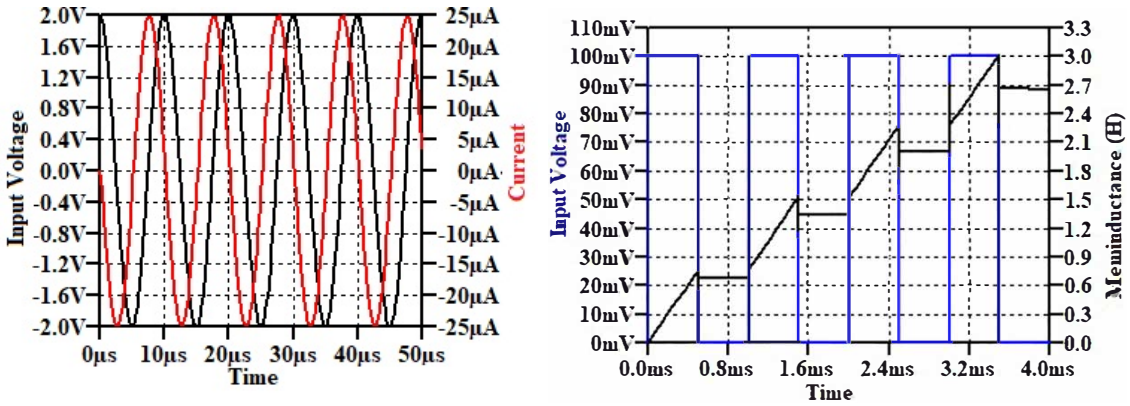
Process corner analysis of the proposed circuits is conducted to assess the variation in circuit performance due to manufacturing process variations. It involves testing circuits under different process corners. These corners are (i) fast-fast (FF), (ii) fast-slow (FS), (iii) slow-fast (SF), and (iv) slow-slow (SS). Figure 12 depicts the results of the corner analysis and verifies that the proposed circuits operate satisfactorily in a complete workspace.

The temperature analysis has been done to evaluate the performance of the proposed circuits under varying thermal conditions. The temperature is varied in the range of -40 °C to +40 °C. The results obtained are displayed in Figure 13. Figure 13 demonstrates that the pinched hysteresis curves exhibit no deformation and confirm satisfactory performance with temperature variations.



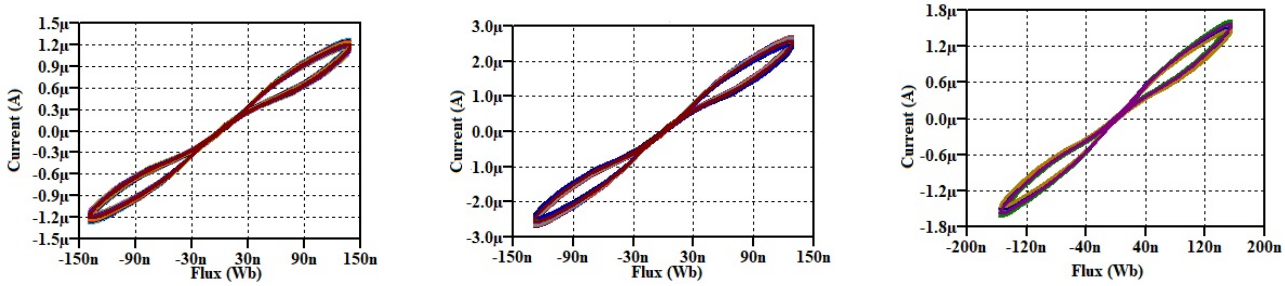
(a) (b) (c)

Figure 9. Pinched hysteresis loops of the proposed circuits depicted in Figures 2a, 2b, and 2c respectively using memristor emulator.



(a) (b)

Figure 10. (a) Time domain response and (b) Nonvolatile nature for the proposed circuit of Figure 2a.

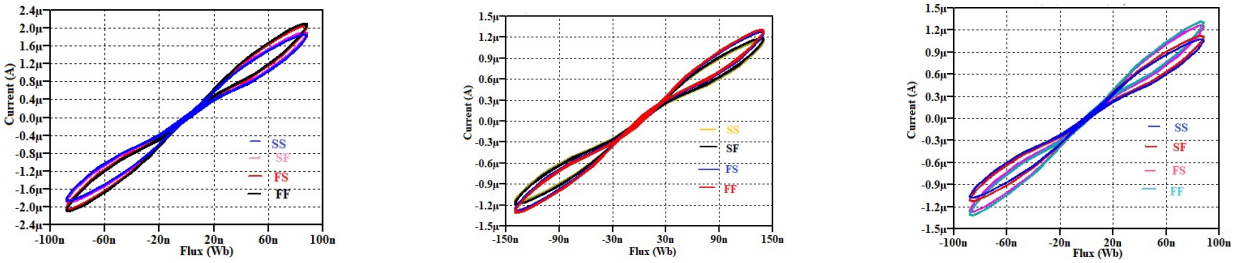


(a) (b) (c)

Figure 11. Monte Carlo Simulation of the proposed circuits depicted in Figures 2a, 2b, and 2c respectively.

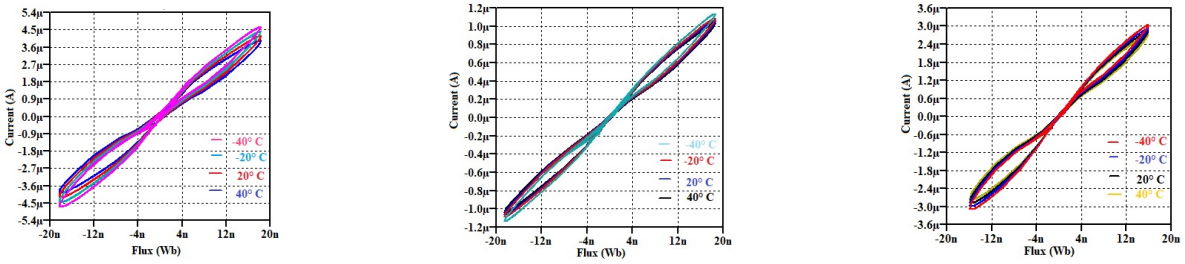
5. Comparison of the meminductor circuits

The traits of the proposed meminductor are contrasted with the traits of the circuits of the meminductor presented in the literature. The comparison considers a variety of aspects such as count of active blocks, count of passive elements, DC supply voltage, working frequency range, configuration of the meminductor emulator, technology used, and power consumption. From the investigation of Table 2, the following conclusion can be drawn:



(a) (b) (c)

Figure 12. Corner analysis of the proposed circuits depicted in Figures 2a, 2b, and 2c respectively.



(a) (b) (c)

Figure 13. Pinched hysteresis loops of the proposed circuits depicted in Figures 2a, 2b, and 2c respectively for different temperatures.

1. It is evident from the referenced circuits in Table 2, that the proposed meminductor circuits operate at a low DC supply voltage of ±0.9 V.

2. The meminductor emulators discussed in Table 2 operate in Hz or a few tens of kHz frequency range [17, 19–22, 24, 25, 27, 30–32] and our proposed designs operate up to 1 MHz frequency range.

3. The proposed circuits are realized utilizing one CMOS-based operational amplifier and seven passive components whereas the circuits of the emulator presented in Table 2 require the complex block such as current conveyors, voltage differentiators, and current feedback amplifier for their realization which makes their practical realization expensive [19–21, 25, 30, 35, 37]

4. The meminductor emulator circuits reported in [19–21, 25, 27, 28, 30–33], realized employing an analog multiplier that results in complex and bulky designs whereas the proposed meminductor circuits do not require any multiplier for their realization which makes them simple and easy to realize.

5. The power consumption of the proposed circuit is greater than that of [28, 34] and smaller than that of [39]. However, the proposed design requires fewer active building blocks compared to these designs.

6. Applications

Two applications namely chaotic oscillator and high pass filter are presented in this paragraph to display the workability of the proposed meminductor circuit.

Table 2. Comparison with previous works.

Refs.	Number of active blocks	Number of passive components	DC supply voltage	Frequency range	Floating/ Grounded (F/G)	Tech. used (nm)	Power consumption (W)
[17]	1 Op-amp	1C, 1R, 1M_R	-	Few Hz	G	-	-
[19]	1 Multiplier, 2 CCII, 4 op-amp	2C,7R	±5 V	800 Hz	G	-	-
[20]	1 Multiplier, 3 op-amp, 1 Voltage differentiator	2C,2R,1L	±5 V	300 Hz	G	-	-
[21]	1 Multiplier, 1 Adder, 3 CCII	2C, 3R	±5 V	10 Hz	G	-	-
[22]	1Subtractor, 1 Adder	1C, 1R, 1M_R	±1.25 V	40 Hz	G	-	-
[23]	2 Op-amp	1C, 3R, 1M_R	± 15 V	700 kHz-2 MHz	G	-	-
[24]	1 OTA	1C, 1R,1L	-	500 Hz	G	-	-
[25]	1 OTA,1 Multiplier, 2 CCII, 1 CFOA	2C,7R	±15 V	5 kHz	Both	-	-
[26]	2 op-amp	2M_R,1C, 4R	-	-	G	-	-
[27]	3 CCII,1 Multiplier	2C, 3R	-	5 HZ	Both	-	-
[28]	2 OTAs, 1 Multiplier	2R, 2C	±1.25 V	10 kHz	G	180	2.25m
[29]	3 Op-amp	1C, 8R, 1LED coupled with photoresist	-	10 KHz	F	-	-
[30]	1 Multiplier, 1 DOCCII, 1 CCII	2C, 1L, 2R	±12 V	300 Hz – 700 Hz	G	-	-
[31]	5 Op-amp, 1 multiplier	11 R, 2C	±12 V	200 Hz	F	-	-
[34]	2 OTA, 2 CCII	1R, 2C	±1.2 V	10 MHz	Both	180	1.03m
[41]	2 CDTA	2C	±0.9 V	500 kHz	G	180	-
[35]	1 OTA, 1 CCII, 1 CDBA	1R, 2C	±0.9 V	1 MHz	G	180	-
[40]	1 MVDVTA	1R, 2C	±0.9 V	500 kHz	F	180	-
[36]	2 OTA, 1 CDBA	2C	±0.9 V	2 MHz	Both	180	-
[33]	1 OTA, 1 MO-OTA, 1 multiplier	1R, 2C	±1.25 V	1 MHz	F	180	3.87m

Table 2. (continued)

Refs.	Number of active blocks	Number of passive components	DC supply voltage	Frequency range	Floating/ Grounded (F/G)	Tech. used (nm)	Power consumption (W)
[37]	2 OTA, 1 CDBA	5R, 5C	±0.9 V	3 MHz	Both	180	-
[38]	1 OTA, 1 CCII	1R, 1C, 1L	-	100 kHz	G	-	-
[32]	6 Op-amp, 3 Multiplier	14R, 2C	-	3 kHz	F	-	-
[39]	1 VDTA, 1 DOCCII	1R, 2C	±0.9 V	200 kHz	F	180	8.58m
Proposed	1 Op-amp	1C, 5R, $1M_R$ OR 1C, 4R, $2M_R$	±0.9 V	100 kHz-1 MHz	G	180	4.53m

Op-amp: operational amplifier, CFOA: current-feedback operational amplifier

6.1. Chaotic oscillator

A chaotic oscillator depicted in Figure 14a has been realized using the proposed meminductor. The presented chaotic oscillator is based on Chua's circuit [50]. The chaotic oscillator is implemented with the help of the proposed meminductor (M_L), two capacitors (C_1 and C_2), one inductor (L), one resistor (R), and two negative resistance (-R_1 and -R_2). The negative resistances are realized using operational amplifier based negative impedance converter.

A system of differential equations representing the dynamics of a chaotic oscillator based on a meminductor emulator is given as follows:

$$C_1\frac{dV_1}{dt} = \frac{V_1}{R_1} + \frac{V_1}{R_2} - I_L \tag{30}$$

$$C_2\frac{dV_2}{dt} = I_L - I_{ML} \tag{31}$$

$$L\frac{dI_L}{dt} = V_1 + V_2 - I_L R \tag{32}$$

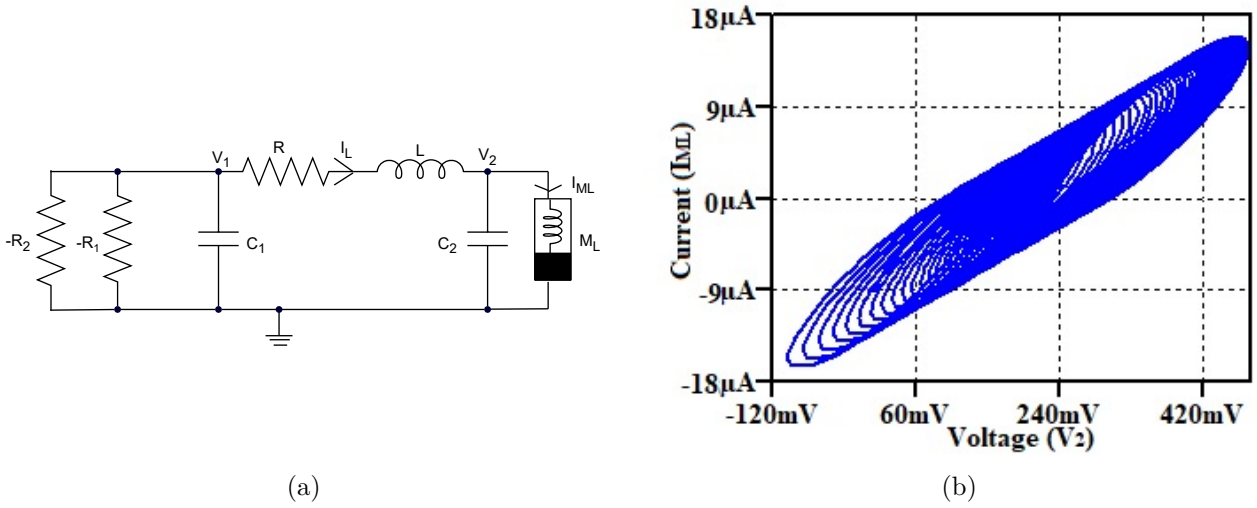
$$M_L\frac{dI_{ML}}{dt} = V_2 \tag{33}$$

The two-dimensional simulation plot for the meminductor-based chaotic oscillator of Figure 14a is displayed in Figure 14b. The values of the components for these plots are $C_1 = 10\ pF, C_2 = 10\ nF, L_1 = 1\ mH$, and $R = 100\ \Omega$. The designed chaotic oscillator can be used in applications such as random number and noise signal generators.

6.2. High pass filter

The applicability of the proposed meminductor has been validated by realizing a second-order high pass filter shown in Figure 15a. The transfer function of the filter is represented in (34)

$$H(s) = \frac{s^2}{s^2 + \frac{1}{M_L C} + s\frac{R}{M_L}} \tag{34}$$



(a) (b)

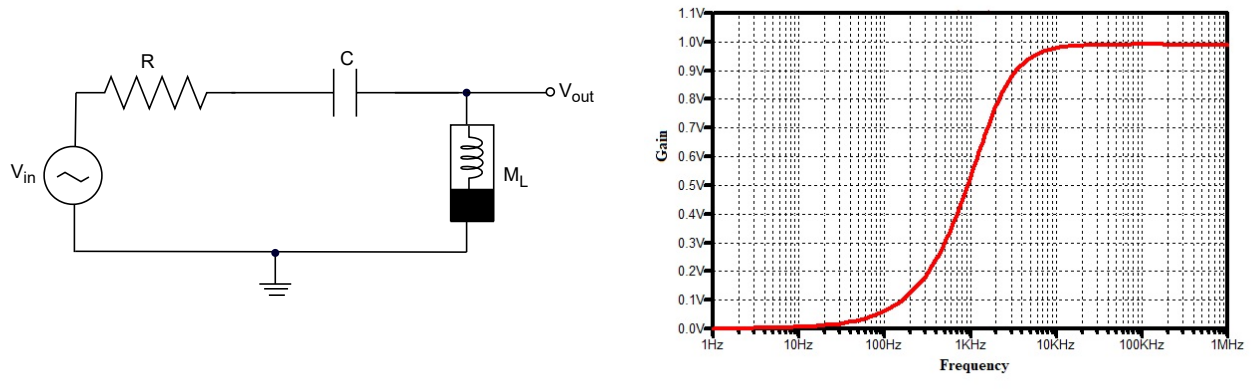
Figure 14. (a) Proposed meminductor based Chaotic oscillator (b) its 2-D output plot.

The filter's resonance frequency and quality factor are as follows:

$$W_0 = \frac{1}{\sqrt{M_L C}} \tag{35}$$

$$Q = \frac{W_0 M_L}{R} \tag{36}$$

To check the workability of the second-order high pass filter, it is simulated using LTspice by choosing the value of $C = 5\ nF$, $R = 100\ \Omega$ and replacing the passive inductor by the proposed meminductor as depicted in Figure 15a. Figure 15b depicts the frequency response of the filter. The -3db frequency of this second-order high pass filter is 1.6 KHz obtained from the graph.



(a) (b)

Figure 15. (a) Proposed meminductor based second-order high pass filter (b) Frequency response of the filter.

7. Experimental validation of proposed meminductor mutator

The functionality of the proposed meminductor depicted in Figure 2a has been confirmed through the experimental setup depicted in Figure 16. The proposed circuit has been realized using an operational amplifier and a memristor emulator. Therefore, an operational amplifier has been realized utilizing the Texas Instruments LM324 IC. The power supply used for IC LM324 is ±15 V. The values of passive components are chosen as $R_1 = R_2 = R_3 = 20\ k, R_5 = 7\ k, R_6 = 1.5\ k$, and capacitance of 1.08 nF. The memristor emulator of Figure 5 is implemented using four ALD1116 n-channel MOSFET ICs and a capacitor of value 0.22 µF. The pinched hysteresis loop obtained for a frequency of 94 kHz using the implemented circuit of Figure 16 is depicted in Figure 17. The performance has been tested using the SPICE models of LM324 and ALD1116.

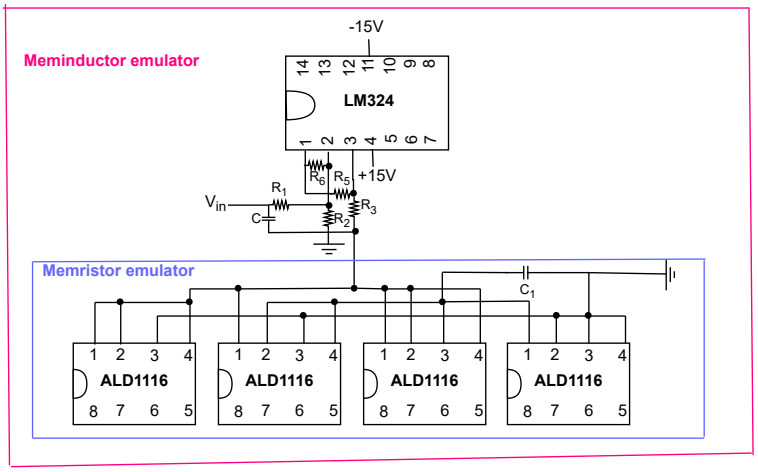


Figure 16. Experimental setup of the proposed circuit depicted in Figure 2a.

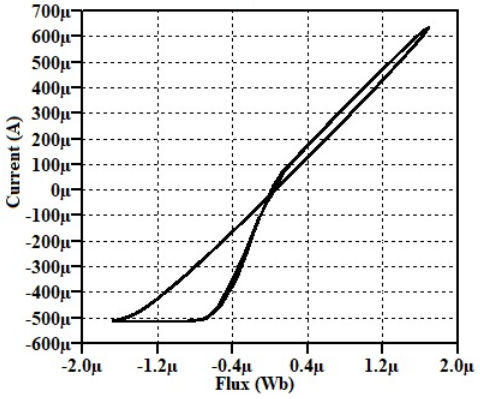


Figure 17. Pinched hysteresis loop obtained through the implemented circuit of Figure 16.

8. Conclusion

This paper presents a new design of meminductor circuits implemented utilizing a single operational amplifier, capacitor, resistor, and memristor. The proposed circuits mutate the dynamics of memristive systems into an efficient meminductive response. Contrary to previous designs that have been presented in the literature, the

proposed circuits have a simple structure. The nonlinear dopant drift SPICE model of memristor and CMOS-based operational amplifier is used for performing all simulations. The workability of proposed circuits is also verified using a memristor emulator circuit. All the simulations are done on the LTspice tool utilizing 180 nm CMOS process technology parameters. The proposed meminductor circuits operate well within a frequency range of up to 1 MHz. SPICE simulation is done to confirm the proposed circuit's nonvolatile characteristic. The practicability of the proposed circuit has been confirmed by implementing a chaotic oscillator and a second-order high-pass filter.

Conflict of interest

The authors declare that they have no conflict of interest.

Author contributions

All authors contributed towards the conception of the idea and circuit design. All authors contributed to material preparation, data collection, circuit designs, simulations, and analyses. All authors read and approved the final manuscript.

References

[1] Chua L. Memristor-the missing circuit element. IEEE Transactions on circuit theory 1971; 18 (5): 507-519. https://doi.org/10.1109/TCT.1971.1083337

[2] Strukov DB, Snider GS, Stewart DR, Williams RS. The missing memristor found. Nature 2008; 453 (7191): 80-83. https://doi.org/10.1038/nature06932

[3] All-Memristor Architecture Could Enable Brain-Like Computers; HRL Labs, Malibu, CA; July 24, 2018.

[4] KNOWM Datasheet Knowm Memristor, March 25, 2019.

[5] Gupta RK, Choudhry MS, Saxena V, Taran S. A Single MOS-Memristor Emulator Circuit. Circuits, Systems, and Signal Processing 2023; 5: 1-20. https://doi.org/10.1007/s00034-023-02500-5

[6] Sözen H, Çam U. Electronically tunable memristor emulator circuit. Analog Integrated Circuits and Signal Processing 2016; 89: 655-63. https://doi.org/10.1007/s10470-016-0785-2

[7] Ananda YR, Raj N, Trivedi G. A MOS-DTMOS Implementation of Floating Memristor Emulator for High-Frequency Applications. IEEE Transactions on Very Large Scale Integration Systems 2022; 31(3): 355-68. http://doi.org/10.1109/TVLSI.2022.3227201

[8] Srivastava P, Gupta RK, Sharma RK, Ranjan RK. MOS-only memristor emulator. Circuits, Systems, and Signal Processing 2020; 39: 5848-61. https://doi.org/10.1007/s00034-020-01421-x

[9] Di Ventra M, Pershin YV, Chua LO. Circuit elements with memory: memristors, memcapacitors, and meminductors. Proceedings of the IEEE 2009; 97 (10): 1717-24. https://doi.org/10.1109/JPROC.2009.2021077

[10] Driscoll T, Quinn J, Klein S, Kim HT, Kim BJ et al. Memristive adaptive filters. Applied Physics Letters 2010; 97 (9): 1-3. https://doi.org/10.1063/1.3485060

[11] Hu Z, Li Y, Jia L, Yu J. Chaotic oscillator based on current-controlled meminductor. In: IEEE 2010 International Conference on Communications, Circuits and Systems; Chengdu, China; 2010. pp. 820-823. https://doi.org/10.1109/ICCCAS.2010.5581866

[12] Jo SH, Chang T, Ebong I, Bhadviya BB, Mazumder P et al. Nanoscale memristor device as synapse in neuromorphic systems. Nano letters 2010; 10 (4): 1297-301. https://doi.org/10.1021/nl904092h

[13] Pershin YV, Di Ventra M. Neuromorphic, digital, and quantum computation with memory circuit elements. Proceedings of the IEEE 2011; 100 (6): 2071-80. https://doi: 10.1109/JPROC.2011.2166369

[14] Biolek D, Biolek Z, Biolkova V. PSPICE modeling of meminductor. Analog Integrated Circuits and Signal Processing 2011; 66: 129-37. https://doi.org/10.1007/s10470-010-9505-5

[15] Biolek D, Biolková V, Kolka Z. SPICE modeling of meminductor based on its constitutive relation. In: 10th international conference on instrumentation, measurement, circuits and systems; Venice, Italy; 2011. pp. 76-79.

[16] Biolek D, Biolková V, Kolka Z. Mutators simulating memcapacitors and meminductors. In: IEEE 2010 Asia Pacific Conference on Circuits and Systems; Kuala Lumpur, Malaysia; 2010. pp. 800-803. https://doi.org/10.1109/APCCAS.2010.5774993

[17] Pershin YV, Di Ventra M. Memristive circuits simulate memcapacitors and meminductors. Electronics Letters 2010; 46 (7): 517-518. https://doi.org/10.1049/el.2010.2830

[18] Pershin YV, Di Ventra M. Emulation of floating memcapacitors and meminductors using current conveyors. Electronics Letters 2011; 47 (4): 243–244. https://doi.org/10.1049/el.2010.7328

[19] Sah MP, Budhathoki RK, Yang C, Kim H. A mutator-based meminductor emulator circuit. In: IEEE 2014 International Symposium on Circuits and Systems; Melbourne, VIC, Australia; 2014. pp. 2249-2252. https://doi.org/10.1109/ISCAS.2014.6865618

[20] Sah MP, Budhathoki RK, Yang C, Kim H. Charge controlled meminductor emulator. Journal of Semiconductor Technology and Science 2014; 14 (6): 750-4.

[21] Fouda ME, Radwan AG. Memristor-less current-and voltage-controlled meminductor emulators. In: IEEE 2014 International Conference on Electronics, Circuits and Systems; Marseille, France; 2014. pp. 279-282. https://doi.org/10.1109/ICECS.2014.7049976

[22] Minaei S, Göknar IC, Yıldız M, Yuce E. Memstor, memstance simulations via a versatile 4-port built with new adder and subtractor circuits. International Journal of Electronics 2015; 102 (6): 911-31. https://doi.org/10.1080/00207217.2014.942890

[23] Singh A, Rai SK. Novel meminductor emulators using operational amplifiers and their applications in chaotic oscillators. Journal of Circuits, Systems and Computers 2021; 30 (12): 1-21. https://doi.org/10.1142/S0218126621502194

[24] Babacan Y. An operational transconductance amplifier-based memcapacitor and meminductor. Electrica 2018; 18 (1): 36-8.

[25] Sozen H, Cam U. A novel floating/grounded meminductor emulator. Journal of Circuits, Systems and Computers 2020; 29 (15): 2050247. https://doi.org/10.1142/S0218126620502473

[26] Wang SF. The gyrator for transforming nano memristor into meminductor. Circuit World 2016; 42 (4): 197-200. https://doi.org/10.1108/CW-01-2016-0002

[27] Zhao Q, Wang C, Zhang X. A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit. Chaos: An Interdisciplinary Journal of Nonlinear Science 2019; 29 (1). https://doi.org/10.1063/1.5081076

[28] Konal M, Kacar F. Electronically tunable meminductor based on OTA. AEU-International Journal of Electronics and Communications 2020; 126: 153391. https://doi.org/10.1016/j.aeue.2020.153391

[29] Romero FJ, Medina-Garcia A, Escudero M, Morales DP, Rodriguez N. Design and implementation of a floating meminductor emulator upon Riordan gyrator. AEU-International Journal of Electronics and Communications 2021; 133: 153671. https://doi.org/10.1016/j.aeue.2021.153671

[30] Korkmaz MO, Babacan Y, Yesil A. A new CCII based meminductor emulator circuit and its experimental results. AEU-International Journal of Electronics and Communications 2023; 158: 154450. https://doi.org/10.1016/j.aeue.2022.154450

[31] Setoudeh F, Dousti M. Analysis and implementation of a meminductor-based colpitts sinusoidal oscillator. Chaos, Solitons & Fractals 2022; 156: 111814. https://doi.org/10.1016/j.chaos.2022.111814

[32] Zhai DD, Wang FQ. Simple double-scroll chaotic circuit based on meminductor. Journal of Circuits, Systems and Computers 2020; 29 (03): 2050048. https://doi.org/10.1142/S0218126620500486

[33] Ersoy D, Kacar F. Electronically Charge-Controlled Tunable Meminductor Emulator Circuit with OTAs and its Applications. IEEE Access 2023; 53290–53300. https://doi.org/10.1109/ACCESS.2023.3281200

[34] Shukla G, Kumar P, Paul SK. High-Frequency Tunable Grounded and Floating Incremental-Decremental Meminductor Emulators and Application. Informacije MIDEM 2023; 19: 53 (3). https://doi.org/10.33180/InfMIDEM2023.303

[35] Goel A, Rai SK, Aggarwal B. A New Generalized Approach for the Realization of Meminductor Emulator and Its Application. Wireless Personal Communications 2023; 131 (4): 2501-23. https://doi.org/10.1007/s11277-023-10549-3

[36] Yadav N, Rai SK, Pandey R. New high frequency memristorless and resistorless meminductor emulators using OTA and CDBA. Sādhanā 2022; 47 (1): 8. https://doi.org/10.1007/s12046-021-01785-z

[37] Gupta A, Rai SK, Gupta M. A Fractional-Order Meminductor Emulator Using OTA and CDBA with Application in Adaptive Learning Circuit. Wireless Personal Communications 2023; 131 (4): 2675-96. https://doi.org/10.1007/s11277-023-10566-2

[38] Bhardwaj K, Srivastava M. On the Boundaries of the Realization of Single Input Single Element-Controlled Universal Memelement Emulator. Circuits, Systems, and Signal Processing 2023; 42 (10), 6355–6366. https://doi.org/10.1007/s00034-023-02420-4

[39] Bhardwaj K, Srivastava M. VDTA and DO-CCII based incremental/decremental floating memductance/meminductance simulator: A novel realization. Integration 2023; 88: 139–155. https://doi.org/10.1016/j.vlsi.2022.09.014

[40] Jain H, Aggarwal B, Rai SK. New Modified Voltage Differencing Voltage Transconductance Amplifier (MVDVTA) based Meminductor Emulator and its Applications. Indian Journal of Pure & Applied Physics 2023; 61 (4): 239-46.

[41] Jain H, Rai SK, Aggarwal B. A New Electronically Tunable Current Differencing Transconductance Amplifier Based Meminductor Emulator and its Application. Indian Journal of Engineering and Materials Sciences 2023; 30 (4): 550–558.

[42] Liu Y, Iu HH. Novel floating and grounded memory interface circuits for constructing mem-elements and their applications. IEEE Access 2020; 8: 114761-72. https://doi.org/10.1109/ACCESS.2020.3004160

[43] Yadav N, Rai SK, Pandey R. New grounded and floating memristor-less meminductor emulators using VDTA and CDBA. Journal of Circuits, Systems and Computers 2021; 30(15): 2150283. https://doi.org/10.1142/S0218126621502832

[44] Singh A, Rai SK. OTA and CDTA-based new memristor-less meminductor emulators and their applications. Journal of Computational Electronics 2022; 21 (4): 1026-37. https://doi.org/10.1007/s10825-022-01889-7

[45] Singh A, Rai SK. New meminductor emulators using single operational amplifier and their application. Circuits, Systems, and Signal Processing 2022; 41 (4): 2322-37. https://doi.org/10.1007/s00034-021-01886-4

[46] Gupta A, Rai SK, Gupta M. Grounded Meminductor Emulator Using Operational Amplifier-Based Generalized Impedance Converter and Its Application in High Pass Filter. International Journal of Electrical and Electronics Research 2022; 10 (3): 496-500. https://doi.org/10.37391/ijeer.100316

[47] Pershin YV, Di Ventra M. Memcomputing: A computing paradigm to store and process information on the same physical platform. In: IEEE 2014 International Workshop on Computational Electronics; Paris, France; 2014. pp. 1-2. https://doi.org/10.1109/IWCE.2014.6865809

[48] Di Ventra M, Pershin YV. The parallel approach. Nature Physics 2013; 9 (4): 200-202. https://doi.org/10.1038/nphys2566

[49] Biolek Z, Biolek D, Biolkova V. SPICE Model of Memristor with Nonlinear Dopant Drift. Radioengineering 2009; 18 (2).

[50] Bilotta E, Pantano P. A Gallery Of Chua Attractors. World Scientific 2008. https://doi.org/10.1142/6720