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Active Clamped ZVS Forward Converter With Soft-Switched Synchronous Rectifier

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Abstract

This paper presents the analysis, design and implementation of an active-clamped, ZVS forward converter equipped with a soft-switched synchronous rectifier (ACFC-SR) proposed for high-efficiency, low output voltage dc-dc converter applications. The converter efficiency is maximized due to the soft-switching of the main, active clamp, synchronous rectifier and freewheeling MOSFET switches. The operating principles of the ACFC-SR are analyzed in detail and the converter performance is compared with the alternative forward converter schemes employed in low output voltage dc-dc converters. Experimental results are presented for a converter with a dc input voltage of 48 V, an output voltage of 5 V, and operating at a switching frequency of 120 kHz. An overall power conversion efficiency of 92% is measured at an output power of 50 W. In general, experimental performance results are found to be in good agreement with theoretical ones.

Key Words: *DC-DC converter, forward converter, active clamp, soft switching, synchronous rectifier, magnetic amplifier.*

1. Introduction

The continuous demand in the power supply industry for higher efficiency dc-dc converters at low output voltages drives a need for new power processing techniques and circuit topologies. Several techniques have been proposed for increasing the power conversion efficiency of such converters at high frequencies [1-13]. Among these, resonant (quasi- and multi-resonant) circuit topologies have been chosen for their low switching losses due to the soft-switching of the power transistors and/or the output rectifier [1,3] by taking advantage of the parasitic components. Frequency-controlled resonant converters equipped with a synchronous output rectifier have been proposed in the literature [4] for high efficiency operation at high input and low output voltage applications. With the advances in MOSFET technology, synchronous rectification has become another cost-effective and advantageous tool for maximizing efficiency, especially in power supplies with low output voltages [5-7]. The replacement of the output rectifier Schottky diodes with very-low on-state resistance MOSFETs reduces significantly the conduction losses.

Although resonant mode power conversion achieves low switching loss at high frequencies, besides its complexity of control by frequency modulation, it has the inherent disadvantage of high rms voltage and current stresses on semiconductors causing increased on-state losses compared to PWM converters [8].

Recently, the trend in power processing technology is towards combining the simplicity of PWM converters with the soft-switching characteristics of resonant converters [9-13]. This allows resonant switching of power transistors while the power transfer is through pulse width modulation. Such a constant frequency PWM forward converter with resonant transition has been presented in [9] to achieve zero voltage switching (ZVS) of the primary switch over a wide input voltage range. In addition, the impact of main transformer leakage inductance and circuit parasitic inductances on the low output voltage converters' performance has been discussed in detail [10]. Using MOSFET synchronous rectification on the active clamp forward converter [11], an improvement in efficiency has been achieved as compared to a forward converter with synchronous rectifier using a third winding reset scheme.

In this paper, an active-clamped, ZVS forward converter equipped with a soft-switched synchronous rectifier (ACFC-SR) is proposed for use in some low output voltage applications where, maximized supply efficiency is of utmost importance. A detailed performance analysis and implementation of an active-clamped ZVS forward converter in combination with a soft-switched synchronous rectifier are presented. The operating principles of the converter are analyzed, and the soft switching of the main, active clamp, output synchronous rectifier and freewheeling switches are shown. Performance characteristics of the implemented 50 W ACFC-SR with an input voltage of 48 V, an output voltage of 5 V and, operating at a switching frequency of 120 kHz are given. The performance of ACFC-SR is compared with that of alternative forward converter schemes employed in low output voltage dc-dc converters.

2. Operation Principles of ACFC-SR

2.1. System description

The circuit diagram of the designed active-clamped, ZVS forward converter equipped with a soft-switched synchronous output rectifier is given in Figure 1. The converter's primary side main and auxiliary active clamp switches (Q1 and Q2), and the secondary side freewheeling switch (Q4) can all operate under ZVS conditions whereas the series MOSFET Q3 turns on under zero voltage and zero current (ZVS/ZCS) and turns off under ZVS, thus maximizing the power conversion efficiency. A magnetic amplifier (Magamp) on the secondary side is added to ensure ZVS of the main switch Q1 by preventing the transfer of magnetizing current to the secondary side and to allow ZCS of the synchronous rectifier Q3 at turn-on. The transformer is reset through the clamping capacitor Ccl and the active clamp MOSFET Q2, which is switched complementary to Q1 with a time delay between their gate pulses (Figure 2). The soft-switching of synchronous rectifier switches can be made possible by using the time delay between gate pulses applied to switches Q1Q3 (delay Δt1) and to Q2Q4 (delay Δt2) as indicated in Figure 2, so as to turn-on all MOSFETs losslessly. During time delays, the body diodes of the MOSFETs on the secondary side are conducting. Q4 is turned on and off under ZVS while its body diode was in conduction. Q3, however, is turned on under ZVS/ZCS and turned off under ZVS. To reduce the body diode conduction losses during the delay times and the reverse-recovery losses of the body diodes, the frequency of the converter is chosen relatively low (f = 120 kHz).

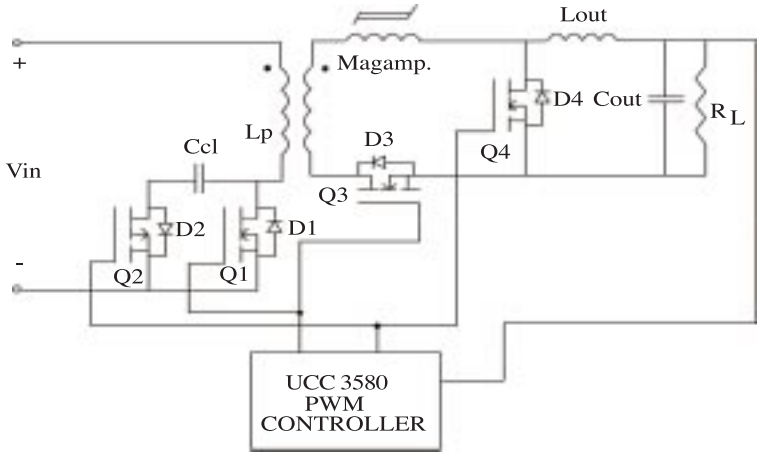


Figure 1. ACFC-SR circuit diagram.

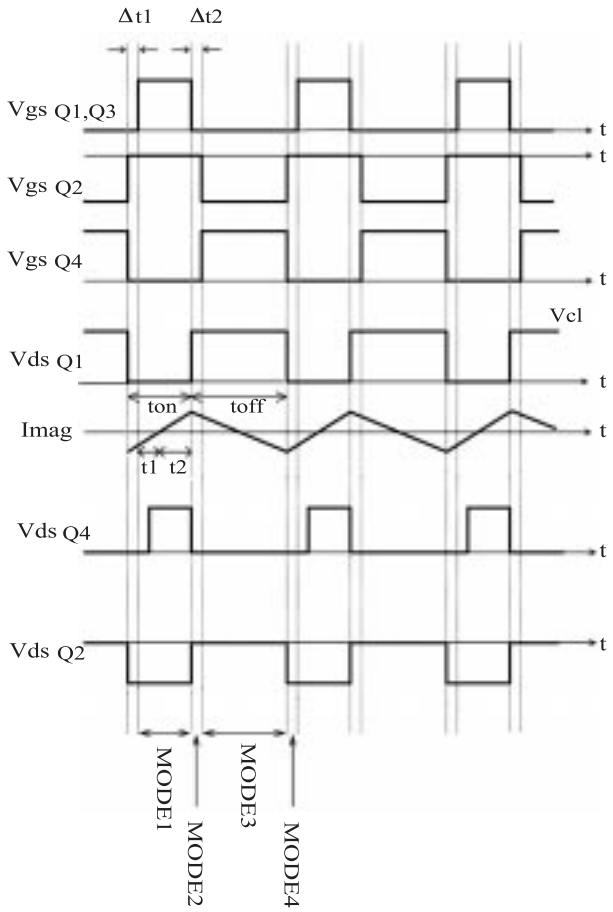


Figure 2. Characteristic waveforms of ACFC-SR.

2.2. Basic operation of ACFC-SR

The ACFC-SR operation can be analyzed in four different modes according to the conduction states of MOSFETs Q1, Q2, Q3 and Q4 and their corresponding intrinsic diodes D1,D2,D3 and D4, illustrated in Table 1. The circuit conditions for each operating mode are given in Figure 3. It is assumed that initially

the intrinsic diodes D1 and D4 are in conduction and the magamp is in blocking state (MODE 4). At time $t = t_0$, Q1 and Q3 receive their gate pulses simultaneously (MODE 1).

Table 1. Conduction states of switches under four possible operating modes.

	Q1	Q2	Q3	Q4	D1	D2	D3	D4	Magamp
MODE 1	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	SAT
MODE 2	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
MODE 3	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	RESET
MODE 4	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF

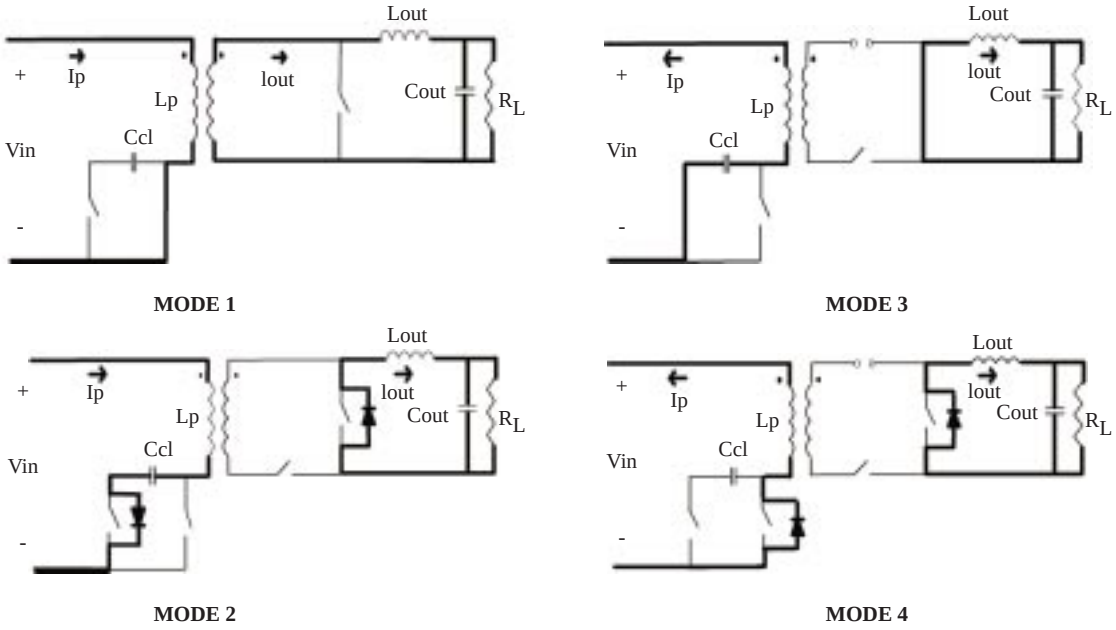


Figure 3. Four operating modes of ACFC-SR.

MODE 1

In this mode, Q1 and Q3 receive their gate pulses simultaneously. Q1 is turned on under zero drain to source voltage since it is switched on while its body diode D1 was conducting. The Magamp was reset in MODE 3, it is now in the blocking state. During the transition period from MODE 4 to MODE 1, only the coercive current of the Magamp, which is much smaller than the output inductor current, flows through the body diode of Q3 and the freewheeling diode D4 continues to carry the load current (Figure 4). Q3 is therefore turned on under zero drain-to-source voltage (ZVS) and nearly zero drain current (ZCS) as illustrated in Figure 5. Due to the simultaneous conduction of D3 and D4, the transformer secondary voltage appears accross the Magamp to move it into saturation. In this way, the Magamp impedance becomes negligible and D3 becomes off. The output inductor current now starts to flow through Q3. Due to the delay caused by the blocking time period of Magamp, the ZVS of Q1 is allowed since the Magamp prevents the flow of magnetizing current in the secondary side. Initially the magnetizing current flows from the source to drain of Q1 (Interval t_1 in Figure 2) and decreases linearly to zero. Then it increases in the opposite direction (Interval t_2 in Figure 2). The primary-reflected load current flows now through Q1.

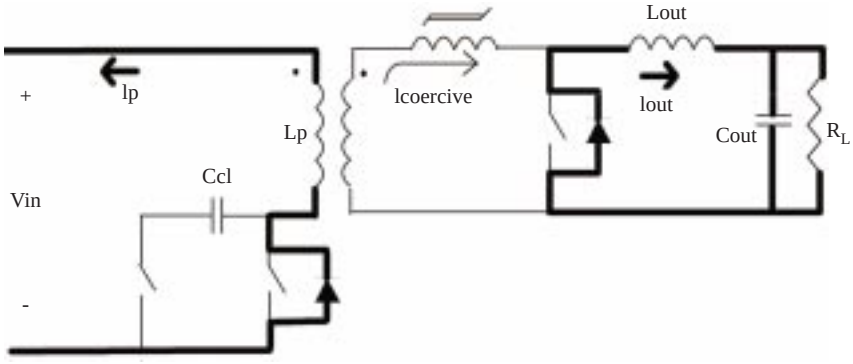


Figure 4. Transition period from MODE 4 to MODE 1.

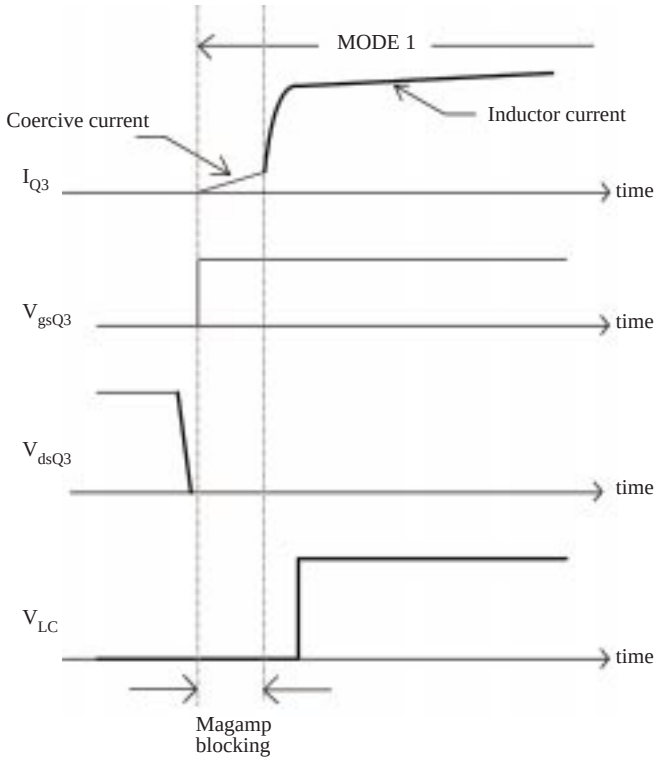


Figure 5. ZCS waveforms of Q3.

MODE 2

At the beginning of MODE 2, the gate pulses of Q1 and Q3 are removed. During the turn-off of Q3, due to the secondary leakage inductance of the main transformer, the load current is first diverted to its body diode D3 (Figure 6). By this method, Q3 is turned off under zero-voltage. Then the current of D3 decays linearly to zero and the load current starts to freewheel through D4. At the turn-off of Q3 and its body diode, the operating point of the Magamp moves from saturation to the residual magnetism level. The Magamp remains in the OFF state during Δt_2 time period (Figure 2). The magnetizing current, which was initially flowing through Q1, is now diverted to the output capacitance of Q1 and then to D2. During MODE 2, voltage across the main switch equals the clamp capacitor voltage Vcl.

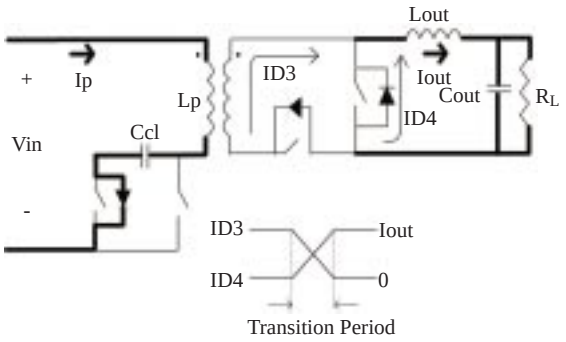


Figure 6. Transition period from MODE 1 to MODE 2.

MODE 3

In this mode, Q2 and Q4 receive their gate pulses. Since D2 and D4 were initially in conduction, ZVS of Q2 and Q4 occurs. The secondary voltage reverses and the Magamp is reset. The reset current flows through the Magamp reset winding via the reset diode and resistor as illustrated in Figure 7. The magnetizing current flows through Q2. It decreases linearly towards zero and then changes its direction. The load current freewheels now through Q4. The transformer is magnetized in the opposite direction and the capacitor Ccl charges and discharges parabolically.

Since the volt-second product applied when Q1 or D1 conduct equals the volt-second product when both Q1 and D1 are OFF, Equation 1 holds true for the clamp capacitor voltage Vcl. The clamp capacitance value is chosen in such a way that the resonant frequency of the LC circuit formed by magnetizing and primary leakage inductance, and the clamp capacitance is much lower than the switching frequency.

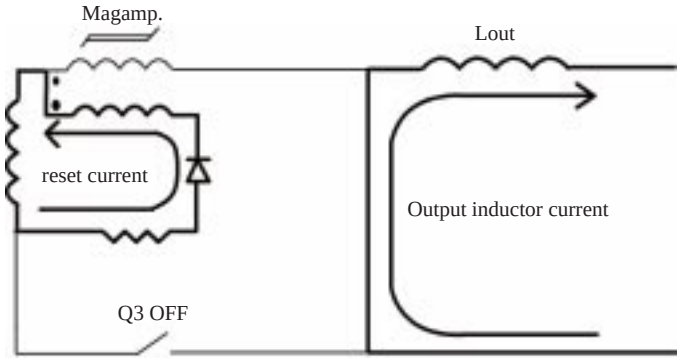


Figure 7. The Magamp reset circuit.

$$Vinton = (Vcl - Vin)toff$$
$$Vcl = VinT/(T - ton) = Vin/(1 - D) \text{ where } D \text{ is duty cycle.} \quad (1)$$

MODE 4

The gate pulses of Q2 and Q4 are removed. The load current, which was freewheeling through Q4 in MODE 3, is now transferred to its body diode D4. Q4 is therefore turned off under ZVS. The magnetizing current flowing through Q2 discharges the parasitic capacitance of Q1 resonatively and then it starts to flow through D1. Since the magamp was reset in MODE 3, it is blocking so that the magnetizing current flows

only in the primary winding. Transition from auxiliary switch Q2 to main switch Q1 is critical. Energy stored in magnetizing and leakage inductances of the main transformer in MODE 4 is used to discharge the parasitic capacitance across the main switch during the time delay Δt_1 (Figure 2). This delay should be optimally programmed at one fourth of the resonance period determined by parasitic capacitance and resonant inductances.

To achieve ZVS of the main switch, energy stored in the magnetizing and leakage inductance must be greater than the energy required to discharge the output capacitance from clamping voltage level down to zero. The output capacitance discharges resonatively to zero as expressed in Equations 2 and 3.

$$1/2LmImag^2 > 1/2CVcl^2 \tag{2}$$

Here, Vcl equals the clamp capacitor voltage which is given by (1). Imag is the peak magnetizing current at the end of reset duration. The output capacitance discharges resonantly to zero.

$$Vcl(t) = Vin - (Vin - Vcl)cos(wt) - Imag\sqrt{\frac{Lm}{C}}sin(wt) \tag{3}$$

where, w is the resonance frequency given by $w = \frac{1}{\sqrt{LmC}}$.

Rearranging (3) gives

$$Vcl(t) = Vin + \frac{(Vcl - Vin)}{cos\Theta}cos\,(wt + \Theta) \tag{4}$$

where $\Theta = tan^{-1}(Imag\sqrt{\frac{L}{C}}/(Vcl - Vin))$

By using (4), it can be shown that for ZVS of the main switch, the following condition must hold:

$$Vcl \geq (1 + cos\Theta)Vin \tag{5}$$

It can be argued that if the initial capacitance voltage Vcl is greater than twice the input voltage Vin (Vcl $>$ 2Vin), zero voltage switching can be achieved regardless of the magnetizing current magnitude. In the case where Vcl is smaller than twice the input voltage (Vcl $<$ 2Vin), a certain amplitude of magnetizing current is required.

3. Design and Implementation of ACFC-SR

3.1. Input-Output specifications

The ACFC-SR is designed and implemented to meet the following input-output specifications:
Nominal input voltage, Vin = 48 V
Input voltage range, ΔVin: 40-60 V
Output voltage, Vo = 5 V
Nominal output current, Io = 10 A
Switching frequency, f = 120 kHz
Efficiency, η = 93% at full-load
Duty cycle at nominal input voltage, D = 30% .

3.2. Design considerations

3.2.1. Power losses

The major components of power losses associated with hard switching PWM dc-dc converters are as follows:

- Conduction and switching losses of the controlled switches
- Conduction and reverse recovery losses of diodes
- Gate drive losses
- Core and copper losses associated with magnetic elements (transformer and output inductor)
- Losses in parasitic elements (associated with the switching element's output capacitance and transformer parasitic capacitance and leakage inductance components)
- Snubber losses
- Output filter capacitor ESR losses

In the ACFC-SR, the switching losses of all MOSFETs are almost eliminated both at turn-on and turn-off (Table 2). The main, freewheeling, and active clamp MOSFETs all turn on under ZVS condition, whereas the synchronous rectifier turns on under both ZCS and ZVS conditions. The main MOSFET has negligible loss during turn-off, due to the nearly ZVS action caused by its high output capacitance. The freewheeling and synchronous rectifier MOSFETs, however, turn off under ZVS. The only losses associated with these switches are therefore the conduction losses depending on the on-state resistance value of the MOSFETs and the forward voltage drop of their body diodes, the reverse recovery losses of body diodes, and the gate drive losses.

The switching frequency of the converter is chosen as 120 kHz so as to keep the reverse recovery loss of the intrinsic diode D4 relatively low. Since all MOSFETs are soft-switched, their output capacitance losses are also eliminated. Furthermore, due to the active clamp action, the energy stored in the leakage inductance of the main transformer is not wasted but used to charge the clamp capacitor for ZVS of the main switch Q1 at turn-on.

Table 2. Soft Switching of all MOSFETs.

ACFC-SR MOSFETs	**Turn-on**	**Turn-off**
Main MOSFET Q1	ZVS	negligible loss
Freewheeling MOSFET Q4	ZVS	ZVS
Synchronous Rectifier Q3	ZCS/ZVS	ZVS
Active Clamp MOSFET Q2	ZVS	negligible loss

A. MOSFET losses

The total power loss associated with the switching elements Q1-Q4 are given in (5).

$$P_{loss(Q1-Q4)} = P_{cond(Q1-Q4)} + P_{cond(D1-D4)} + P_{rcov(D1-D4)} + P_{gate(Q1-Q4)} \tag{6}$$

where conduction losses of MOSFETs and their body diodes can be expressed as

$$P_{cond(Q1-Q4)} = R_{ds(on)} I^2_{Q(rms)} \tag{7}$$

$$P_{cond(D1-D4)} = V_f I_{D(av)} \tag{8}$$

where $I_{Q(rms)}$ and $I_{D(av)}$ denote the rms and average values of the pulsed current waveform respectively and are calculated as

$$I_{Q(rms)} = I_{pft}\sqrt{(t_{on}/T)} \tag{9}$$

$$I_{D(av)} = I_{pft} t'_{on}/T \tag{10}$$

where
I_{pft}: peak flat topped current
t_{on} : conduction time period of the MOSFETs
t'_{on}: conduction time period of the body diodes

$$\Rightarrow P_{loss(Q1-Q4)} = R_{ds(on)} I^2_{Q(rms)} + V_f I_{D(av)} + f V_R Q_f + f Q_{gate} V_{gate} \tag{11}$$

where V_R, V_{gate}, and Q_{gate} denote reverse voltage, gate voltage, and gate charge, respectively.

Q_f is computed from the reverse recovery charge (Q_{rr}), the peak reverse current (I_{rm}) and the slope of the current during turn-off. Typical values for Q_{gate} are specified in the manufacturer's data sheets for different MOSFET types used in this application (Appendix).

$$Q_f = Q_{rr} - I^2_{rm}/(2di_f/dt) \tag{12}$$

Q_f varies usually between 1/2 and 1/4 of the reverse recovery charge Q_{rr}.
Substituting the expressions for $I_{Q(rms)}$, $I_{D(av)}$ and Q_f in (5) yields

$$P_{loss(Q1-Q4)} = R_{ds(on)} I^2_{pft}(t_{on}/T) + V_f I_{pft} t'_{on}/T + f V_R (Q_{rr} - I^2_{rm}/(2di_f/dt)) + f Q_{gate} V_{gate} \tag{13}$$

i- Main MOSFET (Q1)

As the main MOSFET Q1, the IRF3710 Hexfet with an R_{DS}(on) of 28 mΩ is chosen. Since Q1 is turned on under ZVS, it has no turn-on loss. On the primary side, the main MOSFET (Q1) carries both the primary reflected load current and the magnetizing current. Neglecting the magnetizing current and assuming 90% efficiency in the worst case, the rms current of Q1 is estimated as 2.07 A. The conduction loss of Q1 is therefore 0.13 W. The gate drive loss is 0.16 W. Hence, the total loss of the main switch equals 0.29 W since its body diode conduction loss and its reverse recovery losses are negligible.

ii- Active clamp MOSFET (Q2)

A p-channel MTP12P10 type MOSFET is used as the active clamp transistor Q2. The conduction loss of Q2 equals 0.03 W, resulting from the magnetizing current in the reset time interval, which is much smaller than the primary reflected load current. The total loss of Q2 is 0.04 W including the gate drive losses.

iii- Synchronous rectifier (Q3)

An IRF 3205 fifth-generation Hexfet Power MOSFET with an ultra low on-state resistance $R_{DS}(on)$ of $8m\Omega$ is used as the synchronous rectifier Q3. It has no switching loss due to soft-switching at both turn-on and turn-off.

The rms current carried by the synchronous rectifier (Q3) is 5.5 A. Its voltage drop is 80 mV at 10 A, resulting in a conduction loss of 0.24 W. Body diode conduction loss and the reverse recovery losses are calculated as 0.20 W and 0.14 W, respectively. The gate drive losses are 0.14 W. Switching losses are eliminated. Therefore, the total synchronous rectifier loss is 0.72 W.

iv- Freewheeling MOSFET (Q4)

An IRF 3205 MOSFET is also used as the freewheeling MOSFET Q4. Since Q4 is turned on and off while its body diode is in conduction, it has no switching loss. The on-period of Q4 (freewheeling period) equals 5.6 μs. Therefore, the rms current carried by Q4 is calculated as $I_{Q4} = 10\ (5.6/8.0)^{1/2} = 8.4$ A. The conduction loss of Q4 at an output current of 10 A is 0.56 W.

There exists another conduction loss component due to the conduction of the body diode during delay time periods between the gate pulses. The total conduction period of the body diode equals approximately 1 μs (Figure 4). This time period is the sum of the delay times and the blocking time period of the magnetic amplifier, which is necessary for the ZVS of the main switch. The forward voltage drop at 10 A is specified in the manufacturer data sheet as 0.6 V. Therefore, the diode conduction loss is calculated as 0.75 W. Hence, the total loss in the freewheeling MOSFET can be estimated as 1.72 W including the reverse recovery and gate drive losses, which are calculated as 0.27 W and 0.14 W, respectively.

All the power loss components of switches Q1-Q4 at nominal output power are presented in Table 3.

Table 3. MOSFET power losses.

Switches	**MOSFET conduction losses, W**	**Body diode conduction losses, W**	**Reverse recovery losses, W**	**Gate losses, W**	**Total losses, W**
Q1	0.13	negligible	negligible	0.16	0.29
Q2	0.03	negligible	negligible	0.01	0.04
Q3	0.24	0.20	0.14	0.14	0.72
Q4	0.56	0.75	0.27	0.14	1.72

B. Power transformer

The primary and secondary number of turns of the main transformer are chosen as 8:3. A high frequency ferrite core (ETD39- N67 material, ungapped) is used in the power transformer. The transformer core loss is estimated to be 0.35 W for a peak flux density of 45 mT at 120 kHz.

In order to reduce the ac resistance due to skin effect at high frequencies, Litz wire is used in the transformer windings. The primary and secondary winding resistances are measured as 18 $m\Omega$ and 4 $m\Omega$, respectively. The corresponding copper losses are then approximately 0.08 W and 0.12 W. Hence, the total

transformer power loss is 0.55 W.

C. Output filter

Output inductor

An iron powder toroidal core (T157-52 material, ungapped) is used for the output inductor. The inductance value is chosen as 56 μH to satisfy the continuous conduction mode under minimum load conditions, which is usually about 10% of the nominal output current. The measured internal resistance of the inductor is 8 mΩ. This yields a copper loss of 0.80 W at 10 A. Core loss resulting from the ac flux swing is neglected.

Output capacitor

The output filter capacitors were chosen from the low ESR, low ESL, electrolytic type. The output capacitance is Co = 2 x 330 μF having an ESR of 100 mΩ. Since the capacitor rms ripple current is given by ΔI / (2$\sqrt{3}$), the power dissipated by the capacitors equals 40 mW.

D. Magnetic amplifier

The magnetic amplifier used in the circuit is formed by MP1303P-4AS Metglas amorphous alloy 2714A from Allied Signal. At nominal input, the magnetic amplifier must withstand a volt-second product of 18 V for a delay period of 600 ns. From Faraday's equation

V Δt = N Ac ΔB

where

N: the number of turns

Ac: Core cross-sectional area

Δ B: flux swing (ΔB = B_{sat}-B_1, B_1 is the flux density after core is reset).

Metglas 2714A has a saturation flux density of 0.55 T. In order to keep core losses tolerable, the flux swing is kept at 0.88 T with N = 3 turns. The resulting core loss equals 0.11 W. The copper loss is neglected.

For resetting the saturable core, a reverse voltage is applied during the main transformer reset interval. The reset current flows through the reset winding wound on the same core.

$$Hl_c = N_r I_{reset} \tag{14}$$

where H = 4.51 A/m and, l_c = 3.5 cm.

The reset current is 13 mA and the associated power loss in the reset circuit is approximately 0.03 W due to the resistance in the reset path. Therefore, total magnetic amplifier losses are estimated to be 0.14 W.

3.3. Converter efficiency

The losses associated with the switching elements Q1- Q4 (conduction and gate drive losses) and their body diodes (conduction and reverse recovery losses) for the designed ACFC-SR converter with an output power rating of 50 W are given in Table 3. The major loss components of ACFC-SR are MOSFET conduction losses, output inductor losses, power transformer losses and magnetic amplifier losses. The sum of the estimated losses of ACFC-SR equals 3.88 W for an output power of 50 W. The theoretical efficiency is therefore 92.8% at nominal operating conditions.

4. Experimental Results

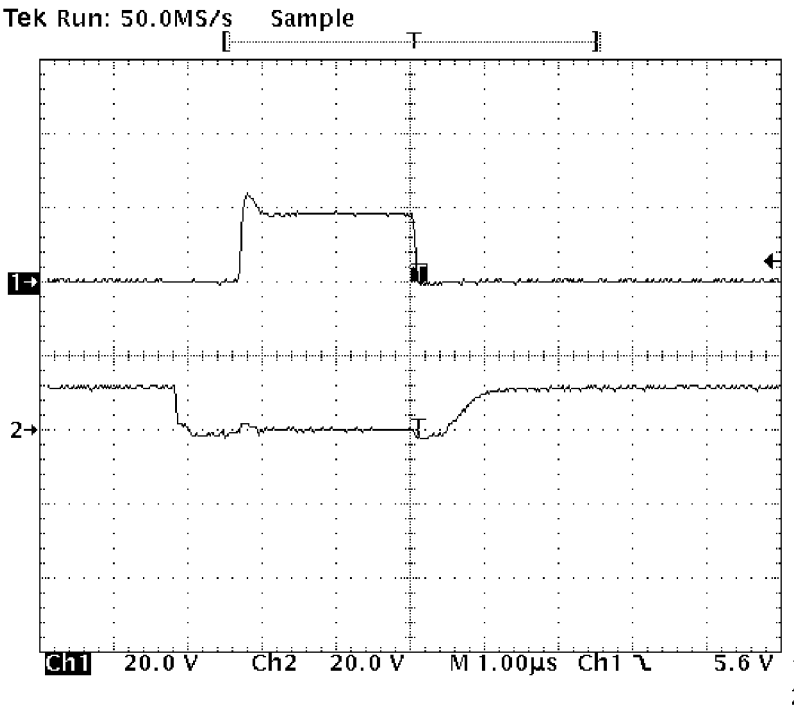
The ACFC-SR converter is implemented and tested for a dc input voltage of 48 V and a dc output voltage of 5V. A dc electronic load (HP6050A) is used to test the ACFC-SR up to a load current of 12 A.

4.1. Performance characteristics of ACFC-SR

The experimental switching characteristics of the four MOSFETs are illustrated in Figures 8 and 9. Figures 8a,b and c show the waveforms of the drain to source voltage and the gate pulses applied to MOSFETs Q4, Q1 and Q3, respectively. It can be observed from these waveforms that gate pulses are applied to the switches at zero voltage, while their body diodes are in conduction. Figures 9, however, illustrates ZCS of Q3. The drain current starts to flow at the end of the blocking time of the magnetic amplifier which ensures Q3 to be turned on at negligibly small current as compared to the load current.

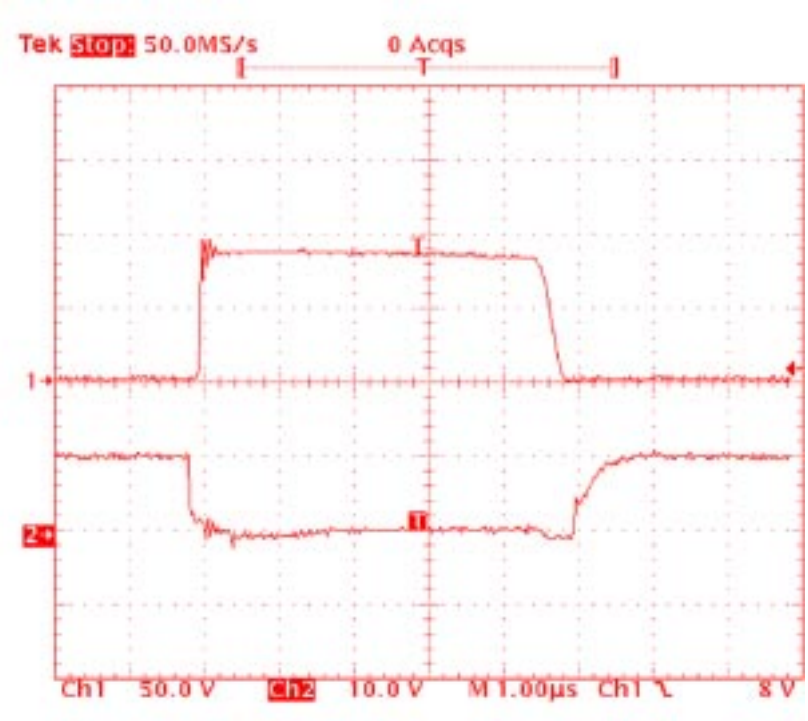
In Figures 10a and 10b, the effect of the magnetic amplifier on the ZVS of the main switch can be seen. The waveforms in Figure 10b are recorded by short-circuiting the magnetic amplifier. In that case, the main MOSFET Q1 cannot be turned on under zero voltage, which causes switching loss.

The efficiency of the ACFC-SR was measured for various load currents at an input voltage of 48 V dc and an output voltage of 5 V dc. The input current is measured using Hall-effect type LEM current transducers. Theoretical and measured efficiencies of the converter are compared in Table 4.



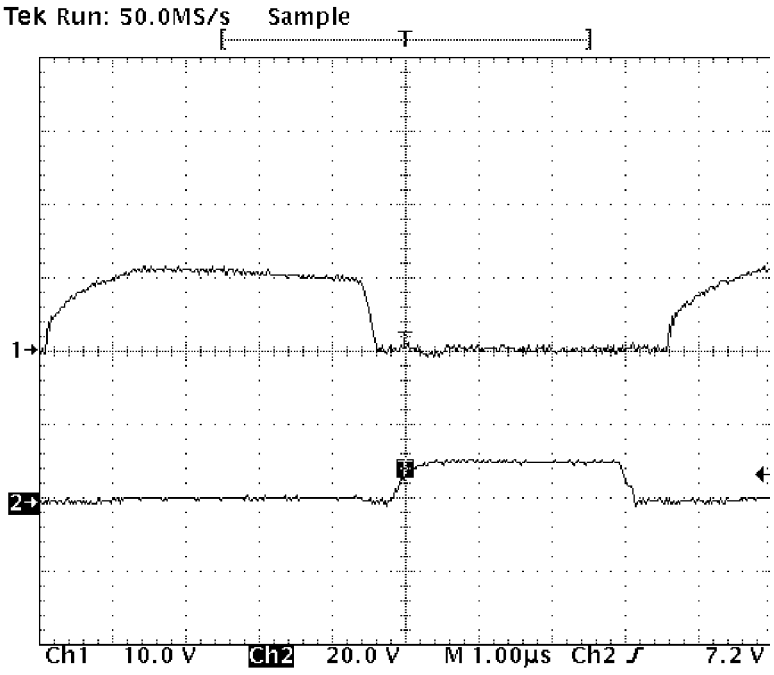
Ch1: Drain to source voltage of Q4, Ch2: Gate to source voltage of Q4

Figure 8a. ZVS waveforms of Q4.



Ch1: Drain to source voltage of Q1, Ch2: Gate to source voltage of Q1

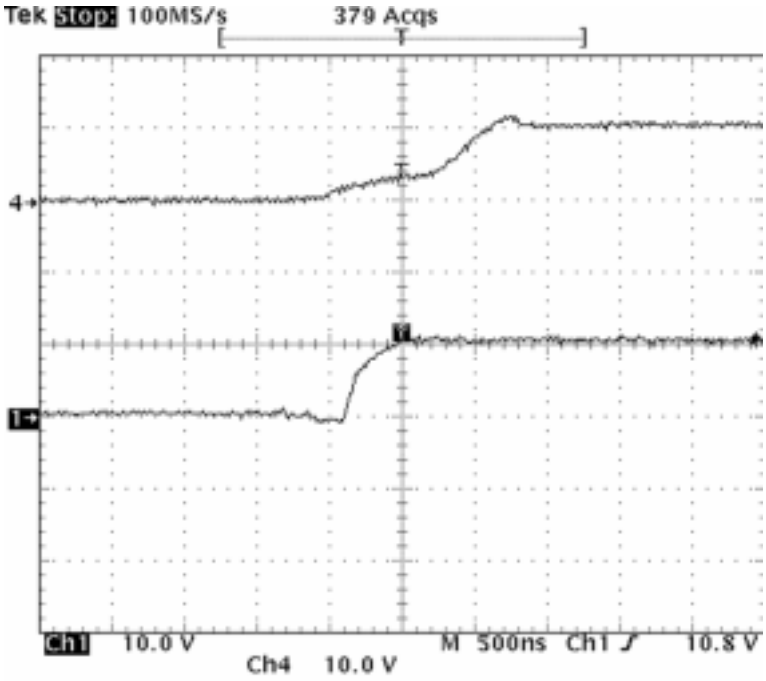
Figure 8b. ZVS waveforms of Q1.



Ch1: Drain to source voltage of Q3, Ch2: Gate to source voltage of Q3

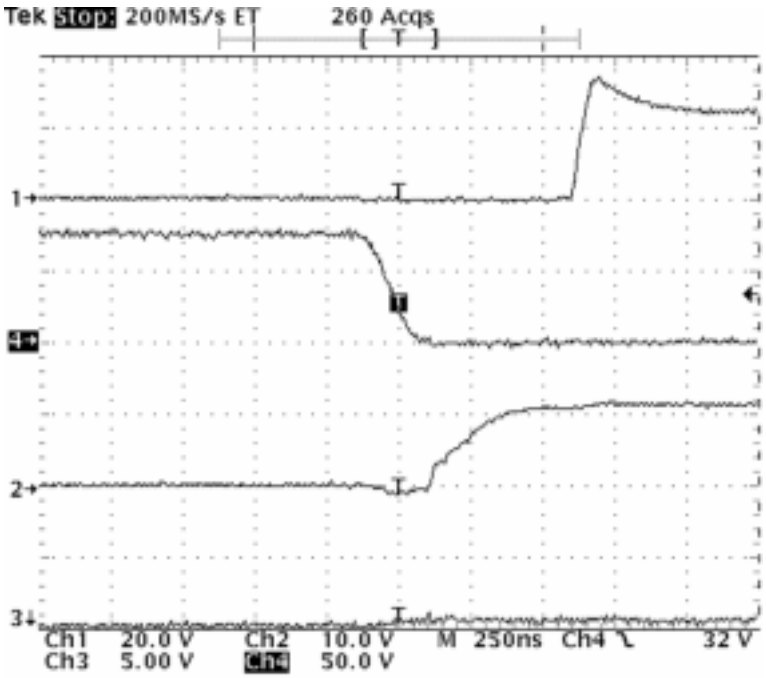
Figure 8c. ZVS waveforms of Q3

Figure 8. Experimental ZVS waveforms of MOSFETs.



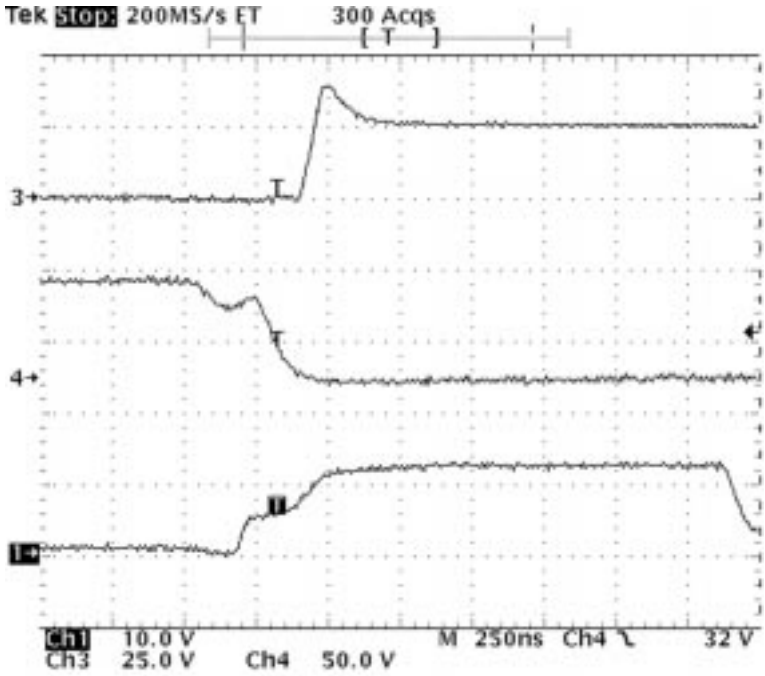
Ch.1: Gate to source voltage of Q3, Ch.4: Drain current of Q3

Figure 9. ZCS waveform of Q3.



Ch1: Input voltage of LC Filter, Ch2: Gate to source voltage of Q1 Ch4: Drain to source voltage of Q1

Figure 10a. Switching waveforms (ZVS) of Q1 and input voltage of LC filter.



Ch1: Gate to source voltage of Q1, Ch3: Input voltage of LC filter Ch4: Drain to source voltage of Q1

Figure 10b. Non ZVS switching waveforms of Q1 after short-circuiting the magnetic amplifier.

Table 4. Theoretical and measured efficiencies of ACFC-SR vs. output current.

Output current, A	**Efficiency, %**	
	Calculated	**Measured**
4	96.7	94.7
6	95.3	94.0
8	93.7	93.1
10	92.8	92.2
12	92.3	91.7

5. Comparison of Alternative Schemes

In this section, alternative schemes employed in low output voltage dc-dc converters with the same input/output characteristics have been compared with the ACFC-SR converter in terms of their power conversion efficiency. These converters are

- **Converter 1:** A standard forward converter having a reset winding with Schottky output rectifiers. Main switch is switched lossy (Non-ZVS).
- **Converter 2:** An active clamp forward converter with Schottky output rectifiers. Main switch is switched lossy (Non-ZVS).
- **Converter 3:** An active clamp forward converter with Schottky output rectifiers and a magnetic amplifier that enables soft switching of the main switch (ZVS).
- **Converter 4:** A standard forward converter having a reset winding with control driven synchronous rectifiers. Main switch is switched lossy (Non-ZVS).

- **Converter 5:** An active clamp forward converter with synchronous rectifiers and a magnetic amplifier. All switches are soft switched (ZVS).

The loss components of alternative forward converters are calculated for an output current of 10 A, and the results are reported in Table 5.

- In the loss comparison of converters,
- Synchronous rectifiers chosen are IRF3205 with Rds(on) = 8 mΩ, and Qrr = 450 nC,
- Schottky rectifiers are 32CTQ030 with Vf = 0.53V,
- Schottky diode reverse leakage current losses are ignored and,
- Synchronous rectifier losses are the sum of conduction losses, body diode reverse recovery losses, and gate drive losses at 120 kHz.

Table 5. Loss comparison of alternative forward type converters.

Losses & Efficiency	**Schottky Rectifiers (W)**	**Synchronous Rectifiers (W)**	**Main MOSFET Switching (W)**	**Mag Amp (W)**	**Leakage Inductance (W)**	***Other Losses (W)**	**Efficiency η (%)**
Converter 1	5.30	-	1.20	-	1.14	1.59	84.42
Converter 2	5.30	-	1.20	-	-	1.59	86.07
Converter 3	5.30	-	-	0.14	-	1.59	87.67
Converter 4	-	2.16	1.20	-	1.14	1.59	89.14
Converter 5	-	2.16	-	0.14	-	1.59	92.79

Other losses include main MOSFET conduction loss, transformer core and copper losses, and output inductor loss.

In the standard forward converter (Converter 1), the energy stored in the leakage inductance of the main transformer is dissipated unlike an active clamped forward converter, which recycles it. Another parasitic loss in hard switched PWM converters occurs due to the discharge of MOSFETs' output capacitance during turn on. These parasitic power losses are not critical at frequencies of a few hundred kHz, but increase with increasing frequency and become significant in SMPS design.

The total transformer leakage inductance referred to the primary side is measured as 1.50 μH. Since inductance is proportional to the square of number of turns, the primary leakage inductance is found as 1.29 μH with a primary-secondary turns ratio of 8:3.

Power dissipation in the leakage inductance is given as

$$P_{lkg} = 0.5 L I_p^2 f \tag{15}$$

where I_p: primary current and equals 3/8 of the output current neglecting magnetizing current
and L: leakage inductance.

This power loss equals 1.14 W at an output current of 10 A and a switching frequency of 120 kHz. The other parasitic loss due to the output capacitance of the MOSFET is neglected since its magnitude is small at 120 kHz. Another loss component is the switching loss of the main switch. The switching loss is given as

$$P_{sw} = V_{in} I_p (t_r + t_f) f/2 \tag{16}$$

where V_{in}: input voltage

t_r: rise time of the gate voltage; t_f: fall time of the gate voltage

t_r and t_f are specified as 59 ns and 48 ns respectively, in the data sheet.

The switching loss is 1.2 W at an input voltage of 48 V, and a switching frequency of 120 kHz.

The second converter does not dissipate the energy stored in the leakage inductance. This results in an increase in efficiency. The other losses remain the same. In the third converter, a magnetic amplifier is added to the secondary side to enable the ZVS of the main switch, which eliminates the switching loss and increases the efficiency further. In the fourth converter, however, Schottky rectifers are replaced with synchronous rectifiers. The high conduction losses of Schottkies are decreased. However, the main MOSFET switching losses and leakage inductance losses do not disappear. The last converter is the active clamped forward converter with synchronous rectifiers. All the switches are soft switched and energy stored in the parasitic elements not dissipated. The high conduction losses of Schottkies are also eliminated by using synchronous rectifiers.

The full-load efficiencies of the alternative forward converters and the ACFC-SR are calculated using the power loss values given in Table 5. The results are reported in Figure 11. The ACFC-SR has the highest efficiency (92.8%) due to synchronous rectification and soft switching of all the switches. The leakage inductance and parasitic capacitance energy is recycled, which improves the efficiency further.

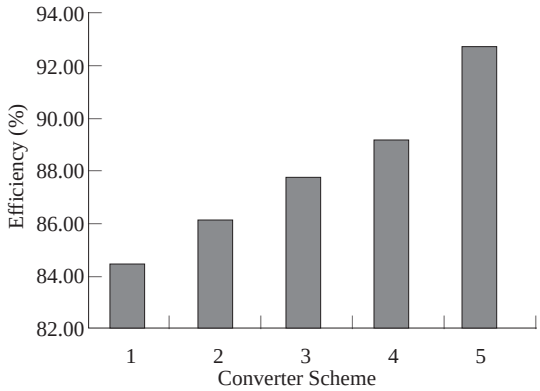


Figure 11. Efficiency comparison of ACFC-SR with alternative forward type converters.

The fourth converter, which uses also synchronous rectifiers instead of Schottkies, has an efficiency of 89.1% due to the elimination of high Schottky conduction losses. However the efficiency achieved is 3.65% lower than that of ACFC-SR, which shows the necessity of active clamping and ZVS of the main MOSFET. The other three converters using Schottky output rectifiers have poorer efficiencies, which is an obvious result of the high conduction losses of Schottky rectifiers. If the magnetic amplifier on the secondary side were removed, the efficiency of ACFC-SR would drop to 91.0% . Therefore, adding a magnetic amplifier for the ZVS of the main switch is critical achieving the high efficiency of ACFC-SR.

6. Conclusions

The operation principles and performance characteristics of a highly-efficient active-clamped ZVS forward converter with soft-switched synchronous rectifier have been presented in detail. The implemented 50 W,

120 kHz ACFC-SR has a measured full-load efficiency of 92.2% due to the integration of a soft-switched synchronous rectifier into an active clamped forward converter. Switching losses of all switches are thereby eliminated and conduction losses minimized. Special attention is paid to the choice of MOSFETs among the fifth-generation ones for minimized Rds(on). Bidirectional use of the transformer, snubberless operation of all switches and the possibility of operating at duty cycles greater than 50% are further advantages of this system.

The efficiencies of alternative buck-derived forward converters are compared with the ACFC-SR. The ACFC-SR has an efficiency 8.3% higher than the standard forward converter with Schottky output rectifiers, and 3.6% higher than the one with synchronous rectifiers, at an output voltage of 5 V, and an output current of 10 A. This scheme can be further used to implement converters operating at lower output voltages such as 3.3 V, which is the trend in new generation microprocessor supplies.

Appendix

Synchronous Rectifier and Freewheeling Power MOSFET ratings:

Code: IRF3205, 5th generation	
Drain to source breakdown voltage, Vdss:	55 V
Continuous drain current at Tc = 25°C, Id:	98 A
Static drain to source on resistance, Rds(on):	8 mΩ
Max. operating junction temperature, Tj:	175°C
Input capacitance at Vgs = 0, Ciss:	4 nF
Output capacitance at Vgs = 0, Coss:	1.3 nF
Body diode forward voltage at Id = 10 A, Vd:	0.6 V
Body diode reverse recovery time:	170 ns max.
Body diode reverse recovery charge:	450 nC at 25°C at If = 9A and di/dt = 100 A/μs

Main MOSFET ratings

Code: IRF 3710, 5th generation	
Drain to source breakdown voltage, Vdss:	100 V
Continuous drain current at Tc = 25°C, Id:	46 A
Static drain to source on resistance, Rds(on):	28 mΩ
Max. operating junction temperature, Tj:	175°C
Input capacitance at Vgs = 0, Ciss:	3 nF
Output capacitance at Vgs = 0, Coss:	0.6 nF

Active Clamp MOSFET:

Code: MTP12P10, p-channel	
Drain to source breakdown voltage, Vdss:	-100 V
Continuous drain current, Id:	12 A

References

[1] K.H. Liu and F.C. Lee, 'Zero Voltage Switching Technique in DC/DC Converters', IEEE PESC'86 Record, June 1986, pp. 58-70.

[2] W.A. Tabisz and F.C. Lee, 'A Novel Zero Voltage Switched Multi-Resonant Forward Converter', HFPC Proceedings, May 1988, pp. 309-318.

[3] F.C. Lee, W.A. Tabisz and M.M. Jovanovic, 'Recent Developments in High Frequency Quasi-Resonant and Multi-Resonant Converter Technologies', Proceedings of EPE, 1989, pp. 368-377.

[4] M.K. Kazimierczuk and C. Wu, 'Frequency-Controlled Series - Resonant Converter with Synchronous Rectifier', IEEE Transactions on Aerospace and Electronic Systems, Vol. 33, No. 3, July 1997, pp. 939-947.

[5] M. Alexander, R. Blanchard and R. Severns, 'MOSFETs move in on low voltage rectification', MOSPOWER Applications Handbook, Siliconix, 1984, 5.87-5.94.

[6] R.A. Blanchard and P.E. Thibodeau, 'The Design of a High Efficiency, Low Voltage Power Supply Using MOSFET Synchronous Rectification and Current Mode Control', IEEE PESC'85 Record, pp. 355-361.

[7] B.E. Taylor, 'High Efficiency Synchronous Rectification with Advanced Fifth Generation HEXFETs', PCIM'95 , Power Conversion Proceedings, pp. 205-210.

[8] K.K. Sum and B.W. Carsten, 'Trends in High Frequency Power Conversion', HFPC Proceedings, May 1988, pp. 1-14.

[9] I.D. Jitaru, 'Constant-Frequency, Forward Converter with Resonant Transition' HFPC Proceedings, June 1991, pp. 282-292.

[10] I.D. Jitaru, 'The Impact of Low Output Voltage Requirements on Power Converters', HFPC Proceedings, May 1995, pp. 1-10.

[11] H.K. Ji and H.J. Kim, 'Active Clamp Forward Converter with MOSFET Synchronous Rectification', PESC'94 Proceedings, pp. 895-901.

[12] I.D. Jitaru and A. Ivascu, 'High-Efficiency Rectification, from State of the Art to Future Trends', PCIM'99, Power Conversion Proceedings, pp. 233 – 245.

[13] A. Açık and I. Çadırcı, 'ZVS PWM Forward Converter with Soft Switched Synchronous Rectifier', PCIM'99, Power Conversion Proceedings, pp. 481-486.

[14] P. Vinciarelli, 'Optimal Resetting of the Transformer's Core in Single Ended Forward Converters', US Patent No: 4441146, April 3, 1984.

[15] B. Carsten, 'Design Techniques for Transformer Active Reset Circuits at High Frequencies and Power Levels', HFPC Proceedings, 1990, pp.235-246.

[16] 'UCC3580 Single Ended Active Clamp/Reset PWM', Unitrode New Product Announcement and Application Information, November 1996.

[17] A.I. Pressmann, 'Switching Power Supply Design', McGraw Hill, 1991.