Turkish Journal of Electrical Engineering and Computer Sciences

Volume 13 | Number 1 Article 5

1-1-2005

Sigma-Delta Voltage to Frequency Converter With Phase Modulation Possibility

MILAN STORK

Turk J Elec Engin, VOL.13, NO.1 2005, © TÜBİTAK

Sigma-Delta Voltage to Frequency Converter With Phase Modulation Possibility

Milan STORK
Department of Applied Electronics, Faculty of Electrical Engineering
University of West Bohemia, UWB, P.O. Box 314 30614 Plzen, Czech Republic
e-mail: stork@kae.zcu.cz

Abstract

Voltage to frequency converter (VFC) is an oscillator whose frequency is linearly proportional to control voltage. There are two common VFC architectures: the current steering multivibrator and the charge-balance VFC. For higher linearity, the charge-balancing method is preferred. The charge balanced VFC may be made in asynchronous or synchronous (clocked) forms. The synchronous charge balanced VFC or "sigma delta" (Σ-Δ) VFC is used when output pulses are synchronized to a clock. The charge balance VFC is more complex, more demanding in its supply voltage and current requirements, and more accurate. It is capable of 16 to18 bit linearity.

In this paper, the New SVFC (NSVFC) is described. This NSVFC works similarly as conventional SVFC but it has a pure tone on output (for constant input voltage). Therefore, it is possible to measure the period of NSVFC output (this does not work for SVFC).

1. Introduction

In recent years, VFC has become quite popular due to their low cost and application versatility in variety of electronic control and measurement systems. With a good quality VFC, this circuit will match the performance of many commercial A/D converters. Its only disadvantage is relatively long conversion time. Σ-Δ modulator [1] can be used for synchronous VFC (SVFC). In SVFC charge balance pulse length is now defined by two successive edges of the external clock. The block diagram of the $\Sigma - \Delta$ VFC is shown on Figure 1. If this clock has low jitter the charge will be defined very accurately. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and they have excellent temperature stability [2], but is not pure tone for constant input voltage (output pulses are not equally spaced). Figure 3 c) shows the waveforms of Σ-Δ SVFC. From Figure 3 c) can be seen that output periods are not the same, but they have changed between 3 and 4 clock cycles. This disadvantage was taken away in NSVFC1 and NSVFC2.

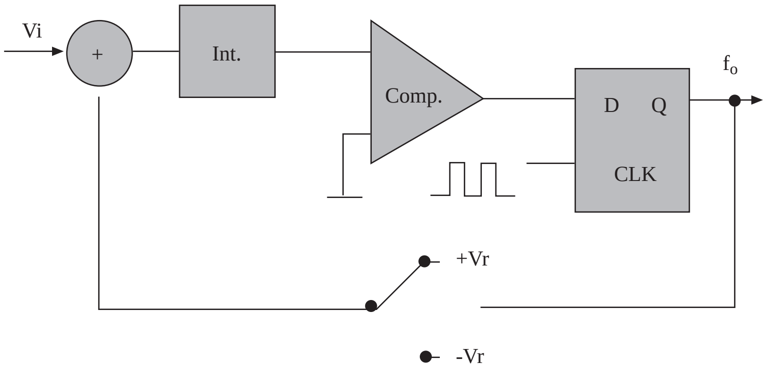

Figure 1. Conventional Σ-Δ voltage to frequency converter (SVFC). Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, D - flip flop.

2. New synchronous Voltage to Frequency Converter

In Figure 2 is NSVFC1 block diagram. Only one-shot is added and connected to comparator output. Figure 3 shows waveforms of this NSVFC1. Number of pulses is same for usual Σ-Δ SVFC [2] and NSVFC (NSVFC1 and NSVFC2).

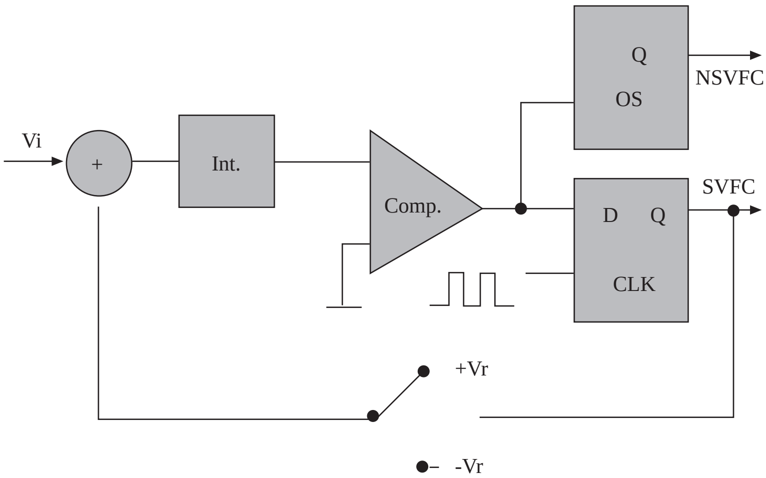

Figure 2. NSVFC1 - New Σ-Δ voltage to frequency converter type1. Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, D - flip flop, OS - one shot.

The output frequency f_O is given by (1):

$$f_O = f_{CLK}(1 - V_i/V_R)/2[Hz, V] \quad (1)$$

where V_i is input voltage, V_R is reference voltage and f_{CLK} is clock frequency. It is important to note, that for NSVFC1 this equation is limited for V_{imin} given by (2). The minimal input voltage value V_{imin}:

$$V_{imin} > 2f_{CLK}V_R t_{dC} \text{ (for NSVFC1) } [V, Hz, sec] \quad (2)$$

where t_{dC} is comparator time delay. E.g. for $f_{CLK} = 10$ kHz, $V_R = 5V$ and $t_{dC} = 200ns$, the minimal value $V_{imin} > 0.02$ V.

3. New synchronous VFC Output Frequency Cetermination

The key to Σ-Δ modulator is the integrator. At each conversion, the integrator keeps a running total of its previous output and its current input. The output from the integrator is feed to 1-bit analog/digital converter (ADC). This is simply a comparator with its reference input at a level of half the input range, 0 V in this case. The ADC output feeds a 1-bit digital/analog converter (DAC) which has output levels equal $+V_R$ or $-V_R$. A summing amplifier completes the loop by summing the current input signal and the previous sample DAC output. The aim of the feedback loop is to try to maintain the average output of the integrator at the comparator reference level, 0 V. Therefore:

$$\sum_{k=1}^{\infty} V_{o1}(k) + \sum_{k=1}^{\infty} V_{o2}(k) = 0 \tag{3}$$

where $k = 1, 2, ...\infty$, and $V_{o1}(k)$ and $V_{o2}(k)$ are integrator output voltage in k output frequency period, see Figure 4. The NSVFC and equivalent period time diagram is shown on Figure 5.

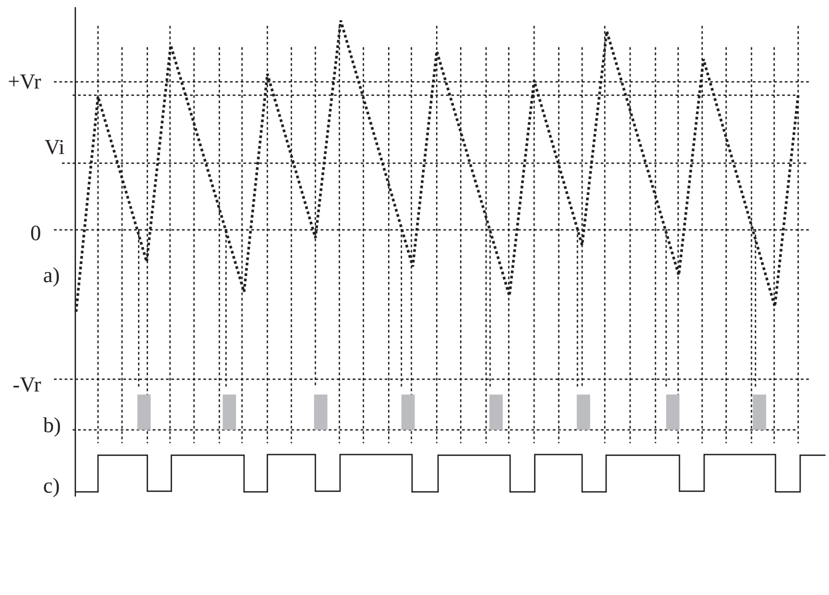

Figure 3. Waveforms of NSVFC. a) integrator output, b) one shot output, c) D-flip flop output. $V_i = 1.8$ V, $V_R = 4$ V, period of one shot is 3.636 T_{clk}.

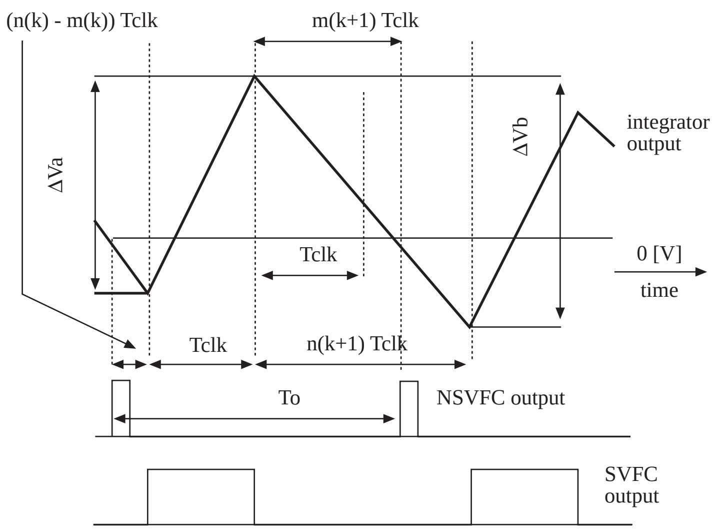

Figure 4. Detailed waveforms of the integrator, D flip-flop SVFC and one shot NSVFC outputs, $n = 2$ in this figure ($nT_{clk} = 2T_{clk}$).

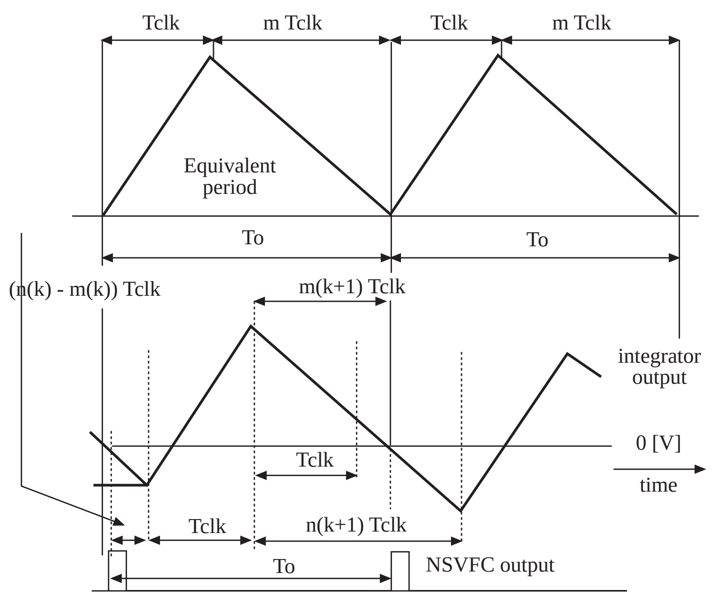

Figure 5. NSVFC waveforms and equivalent period time diagram.

Change ΔV_a is given by (4):

$$\Delta V_a = C \int_0^{T_{clk}} (V_i(t) + V_R)dt \tag{4}$$

and ΔV_b is given by (5):

$$\Delta V_b = C \int_0^{nT_{clk}} (V_i(t) - V_R)dt \tag{5}$$

where C is the integrator constant. The integrator output is given by:

$$V_{o1}(k) = V_{o2}(k-1) + C\int_{0}^{T_{clk}} (V_i(t) + V_R)dt \tag{6}$$

$$V_{o2}(k) = V_{o1}(k) + C\int_{T_{clk}}^{(n+1)T_{clk}} (V_i(t) - V_R)dt \tag{7}$$

and for $V_i(t) = V_i$:

$$V_{o1}(k) = V_{o2}(k-1) + C(V_i + V_R)T_{clk} \tag{8}$$

$$V_{o2}(k) = V_{o1}(k) + C(V_i - V_R)nT_{clk} \tag{9}$$

Integrator output voltage change is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)nT_{clk} \tag{10}$$

where$n$ must be an integer for SVFC. For NSVFC output is given by:

$$C(V_i + V_R)T_{clk} = C(V_i - V_R)mT_{clk} \tag{11}$$

where m is real for NSVFC. From (11) $(V_R > V_i)$:

$$m = \frac{V_i + V_R}{V_R - V_i} \tag{12}$$

and for SVFC, n is given by (13):

$$n = ceil\left(\frac{V_i + V_R}{V_R - V_i}\right) = ceil(m) \tag{13}$$

where Ceil(.) - Converts a numeric value to an integer by returning the smallest integer greater than or equal to its argument. E.g. Ceil(9/3)=3, Ceil(9.01/3) =4.

3.1. Output frequency determination for ideal converter

For this ideal NSVFC it is supposed, that comparator has a zero time delay and noise value voltage on second comparator input is zero. Output period for NSVFC can be determined from Figure 6.

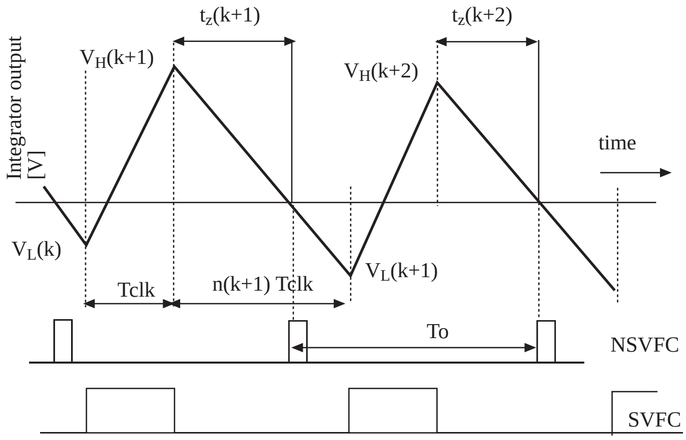

Figure 6. Time diagram for ideal converter - output frequency evaluation.

It is supposed, that $V_R > V_i$, where V_R is reference voltage and V_i is input voltage. The $V_L(i)$ and $V_H(i)$ are voltage at integrator output.

Output period T_0 from Figure 6 is given by:

$$T_0 = T_{clk}[n(k+1) - t_z(k+1) + 1 + t_z(k+2)] \tag{14}$$

Time from $V_L(i)$ to $V_H(i+1)$ is always $1 * T_{clk}$ if no error occurs (error can be caused by comparator delay, comparator hysteresis or voltage change on second comparator input. This will discuss in next part). For $T_{clk} = 1$, the output period T_{01}:

$$T_{01} = n(k+1) - t_z(k+1) + 1 + t_z(k+2) \tag{15}$$

Strait line from $V_L(i)$ to $V_H(i+1)$ has a slope: $V_i + V_R$

The line is given by equation (all following equations are given for $T_{clk} = 1$):

$$V_H(k+1) = V_L(k) + (V_i + V_R).1 \tag{16}$$

The line slope from $V_H(i)$ to $V_L(i+1)$ is: $V_R - V_i$. Line equation is:

$$V_L(k+1) = V_H(k+1) - (V_R - V_i)n(k+1) \tag{17}$$

where $n(k+1)$ is given by:

$$n(k+1) = ceil(V_H(k+1)/(V_R - V_i)) = ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \tag{18}$$

hence

$$\begin{aligned} V_L(k+1) &= V_H(k+1) - (V_R - V_i)n(k+1) \\ &= V_H(k+1) - (V_R - V_i)ceil(V_H(k+1)/(V_R - V_i)) \\ &= V_L(k) + V_i + V_R - (V_R - V_i)ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \end{aligned} \tag{19}$$

The term

$$(V_R - V_i)ceil((V_L(k) + V_R + V_i)/(V_R - V_i))$$

can't be reduced, because *ceil()* is nonlinear function, e.g.: *y(ceil(x/y))* $\neq$ *ceil(x).*

Time $t_z(k)$ is given by:

$$t_z(k) = V_H(k)/(V_R - V_i) \tag{20}$$

Output period equation is given by:

$$\begin{aligned} T_{01} &= n(k+1) - t_z(k+1) + 1 + t_z(k+2) = ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \\ &\quad -V_H(k+1)/(V_R - V_i) + 1 + V_H(k+2)/(V_R - V_i) \end{aligned} \tag{21}$$

After multiplication by term $(V_R - V_i)$, equation (21) is changed to:

$$\begin{aligned} (V_R - V_i)T_{01} = (V_R - V_i)ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) - (V_L(k) + V_R + V_i) + \\ +V_R - V_i + V_L(k+1) + V_R + V_i \end{aligned} \tag{22}$$

$V_L(k+1)$ is substitute by equation (19), hence:

$$\begin{aligned} (V_R - V_i)T_{01} &= (V_R - V_i)ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) - (V_L(k) + V_R + V_i) + \\ &\quad +2V_R + V_L(k) + V_i + V_R - (V_R - V_i)ceil((V_L(k) + V_R + V_i)/(V_R - V_i)) \end{aligned} \tag{23}$$

After reduction, output period T_{01} is given by:

$$T_{01} = 2V_R/(V_R - V_i) \tag{24}$$

and output frequency f_{01} hence:

$$f_{01} = (V_R - V_i)/2V_R \tag{25}$$

and for $T_{clk} \neq 1$ the output frequency f_0:

$$f_0 = f_{clk}(V_R - V_i)/2V_R \tag{26}$$

where $f_{clk} = 1/T_{clk}$

From (26) is shown, that ideal NSVFC output frequency is linearly dependent on input voltage (f_{clk} and V_R are constants).

3.2. Output frequency determination for real converter

Now, error caused by comparator delay, comparator hysteresis or voltage change on second comparator input is described. This error is displayed on Figure 7 and is sign by X point. The error can arise especially when input voltage $V_i \approx 0$. The error occur when 2 clock cycles are need for $V_L(k)$ to $V_H(k+1)$ transition. In this case, this must be detected and output pulse is generated. When integrator output voltage on one comparator input is greater than voltage on second comparator input (it is important to note, that in ideal condition, output pulse is generated only when voltage on integrator output is lower then voltage on second comparator input - leading edge of integrator output). The additional logic is used for this purpose. The block diagram of this NSVFC2 is shown in Figure 8.

Output period T_{e1} from Figure 7 is given by:

$$T_{e1} = T_{clk}[n(k) - t_z(k) + t_e(k)] \tag{27}$$

For $T_{clk} = 1, V_i << V_R$ output period T_{e11} is given by:

$$T_{e11} = ceil(V_H(k)/(V_R - V_i)) - V_H(k)/(V_R - V_i) + |V_L(k)/(V_R + V_i)| \tag{28}$$

In (28) $ceil(V_H(k)/(V_R - V_i)) = 2$ and $V_H(k) \approx V_R$ and $|V_L(k)| \approx V_R$ for $V_i \approx 0$. Hence:

$$T_{e11} = 2 - V_R/(V_R - V_i) + V_R/(V_R + V_i) \approx 2(1 - V_i/V_R) \tag{29}$$

Similarly the output period T_{e21} is given by:

$$\begin{aligned} T_{e21} &= 2 - t_e(k) + V_R/(V_R - V_i) \qquad (30) \\ &= 2 - V_R/(V_R + V_i) + V_R/(V_R + V_i) \approx 2(1 + V_i/V_R)X(30) \end{aligned}$$

Equations (29) and (30) for $T_{clk} \neq 1$ are simplified to:

$$T_{e1} \approx 2T_{clk}(1 - V_i/V_R) \tag{31}$$

$$T_{e2} \approx 2T_{clk}(1 + V_i/V_R) \tag{32}$$

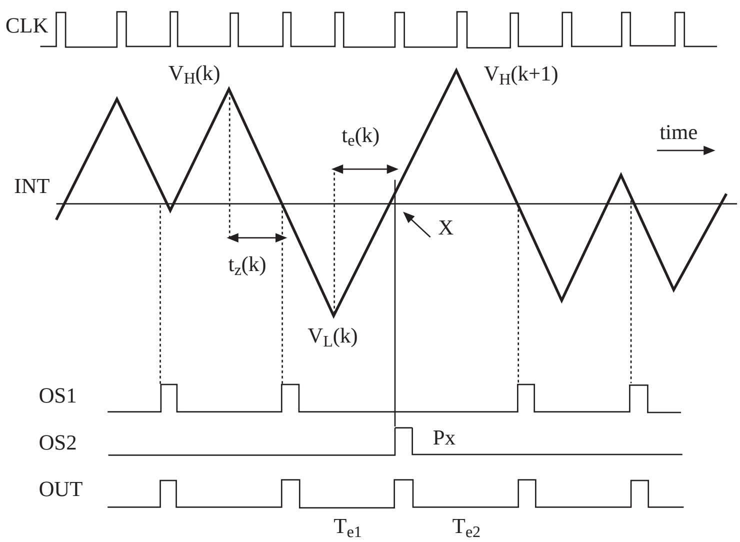

Figure 7. Time diagram for real converter - output frequency evaluation.

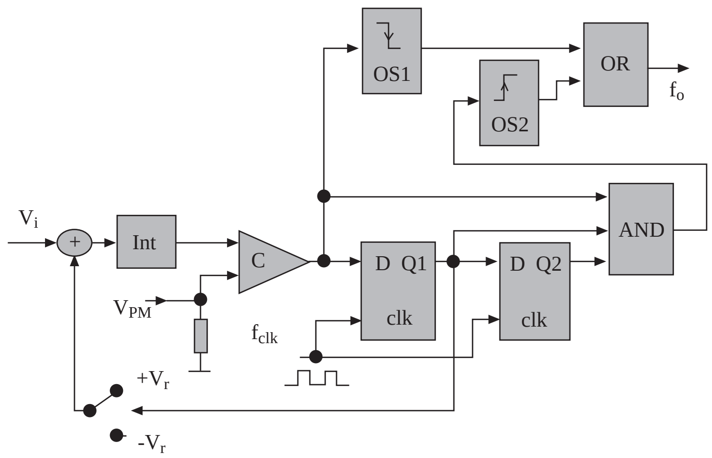

Figure 8. NSVFC2 - Block diagram. Int. - integrator, Comp. - comparator, V_i - input voltage, V_R - reference voltage, V_{PM} - input voltage for phase modulation, D - flip flop, OS - one shot, AND, OR - log. function.

4. Possibility of Phase Modulation

The NSVFC2 has phase modulation capabilities. When the modulating voltage V_{PM} is applied to second comparator input, see Figure 8, the output signal is phase modulated. The $V_{PM} < V_R$ must be satisfied for modulation voltage. The time diagram for phase modulation computing is shown on Figure 9. The example of phase modulation simulation is shown in Figure 10.

For$T_{clk} = 1$, the output period T_{PM1} is given by (33):

$$T_{PM1} = n(k+1) - t_z(k+1) + 1 + t_{zPM}(k+2) \tag{33}$$

The equation for $n(k+1)$ and $t_z(k+1)$ are the same as (18) and (20). But $t_{zPM}(k+2)$ is:

$$t_{zPM}(k+2) = (V_H(k+2) - V_{PM})/(V_R - V_i) \tag{34}$$

where V_{PM} is voltage on second comparator input.

After some mathematics manipulation the T_{PM1} is:

$$T_{PM1} = (2V_R - V_{PM})/(V_R - V_i) = 2V_R/(V_R - V_i) - V_{PM}/(V_R - V_i) = T_{o1} - \Delta T_{PM1} \tag{35}$$

hence $\Delta\varphi$ is given by (36):

$$\Delta\varphi = \pi V_{PM}/V_R \qquad [rad, V] \tag{36}$$

From (36) is shown, that NSVFC2 phase change is linearly dependent on input voltage V_{PM}.

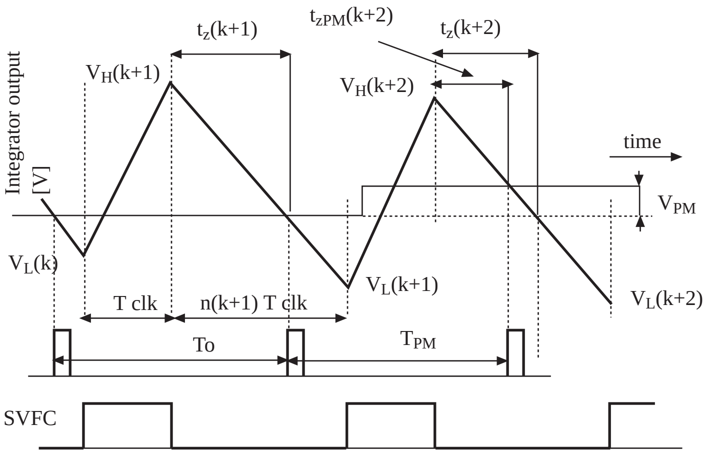

Figure 9. Time diagram for phase modulation evaluation.

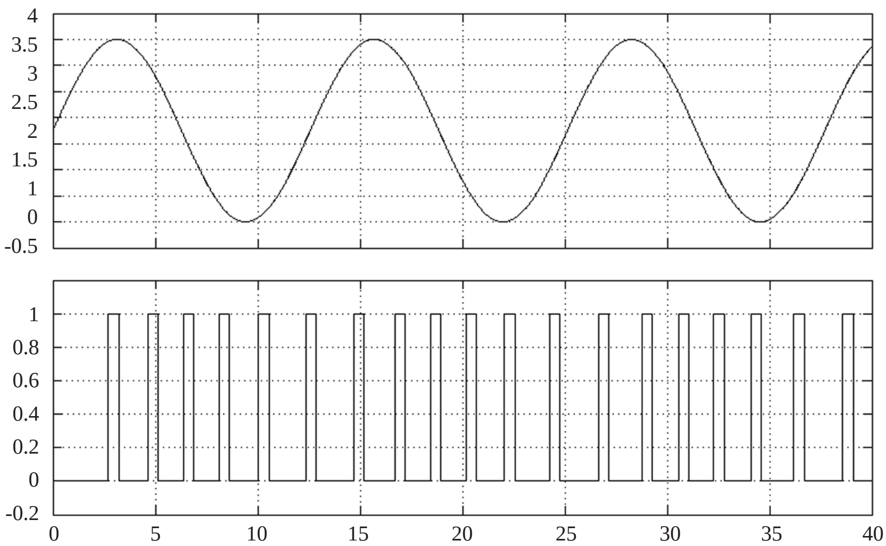

Figure 10. Example of phase modulation (simulated).

5. SVFC Simulation Results

Simulations were performed to validate the results of mathematics analysis. These results were obtained programming of SVFC and NSVFC equations (Figure 3). The SVFC, NSVFC1 and NSVFC2 has also been simulated in system level by SIMULINK (MATLAB). The block diagram of this simulation is shown in Figure 11. The simulated waveforms are shown in Figure 10 and 12. Figure 13 shows the frequency spectrum of the output waveforms from Figure 12. Figure 14 shows the waveforms with errors, which are corrected by additional logic used in NSVFC2.

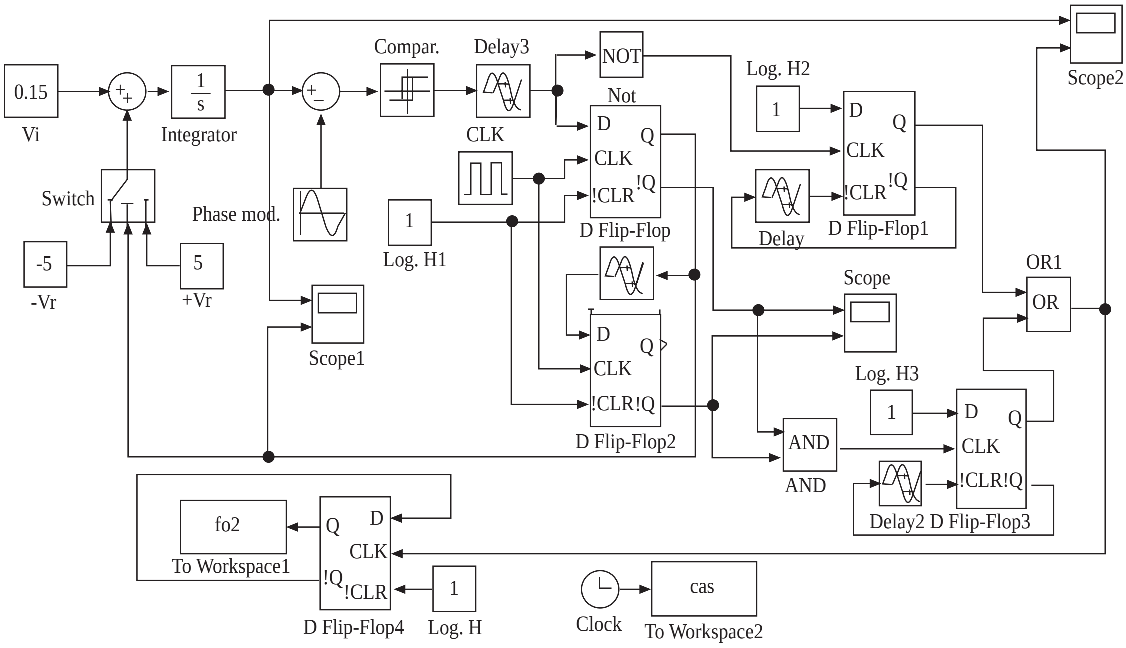

Figure 11. NSVFC2 block diagram for simulation.

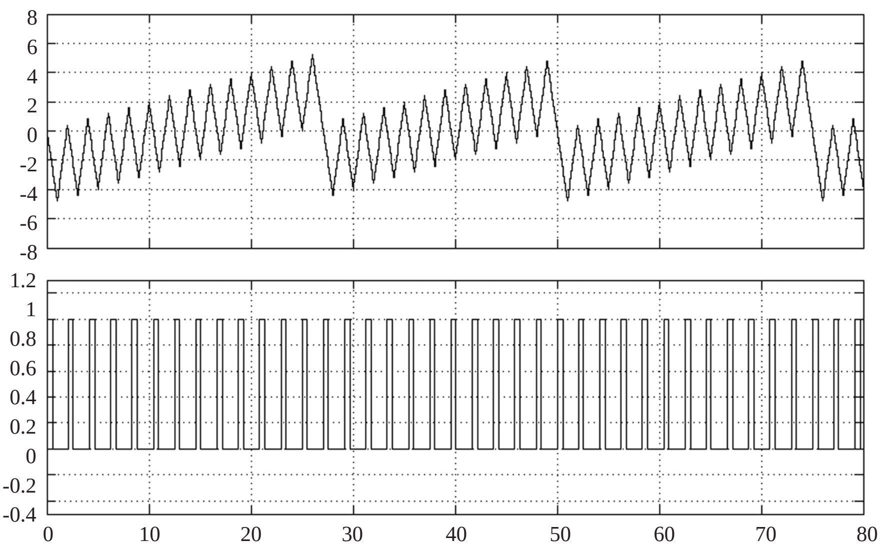

Figure 12. Simulated waveforms (no errors).

6. Experimental Results

Commercially produced SVFC AD7741 and AD7742 [2] were tested and also NSVFC1 was realized and tested [12], [15]. In Figure 15, experimentally realized NSVFC1 simplified circuit diagram is shown [3]. The voltage/frequency characteristic and frequency spectrum was measured. In Figure 16, graph of measured voltage/frequency characteristic of experimental NSVFC1 is shown. In Tab. 1, some measured values V_i a f_o are displayed. In Figure 17, the oscilloscope photograph shows the integrator output and D-flip flop output of SVFC. In Figure 18, the oscilloscope photograph shows also integrator output and one shot output of NSVFC1. In common type of SVFC, since the output pulses are synchronized to a clock they are not equally spaced (Figure 17). This need not affect the user of a SVFC for A/D conversion, but it does prevent its use as a precision oscillator. Despite this disadvantage the improvement in performance makes the SVFC ideal for the majority of high-resolution VFC applications.

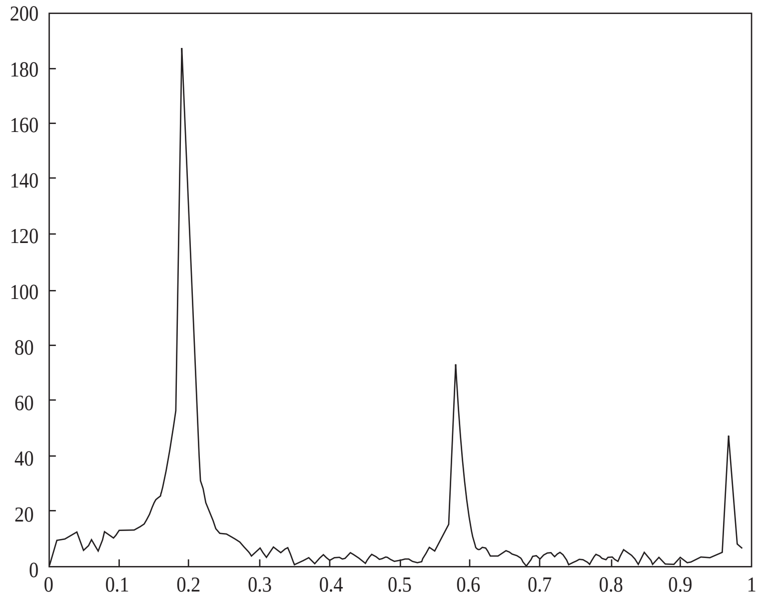

Figure 13. Frequency spectrum of waveforms from Figure 12.

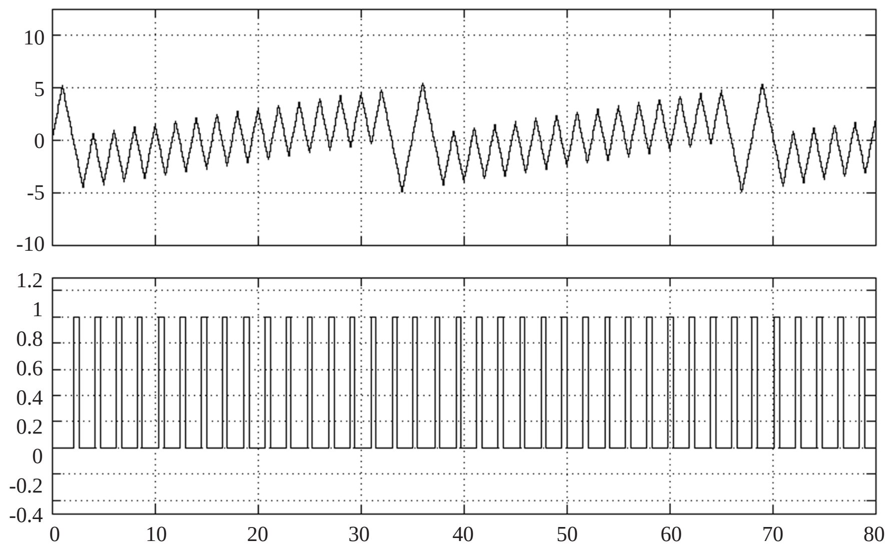

Figure 14. Simulated waveforms (with errors). Errors are corrected by logic, added to NSVFC2.

In Figure 19, the frequency spectrum of SVFC is shown and in Figure 20, the spectrum of NSVFC1 is displayed. From Figure 20 can be seen, that spurious spectral lines are rejected.

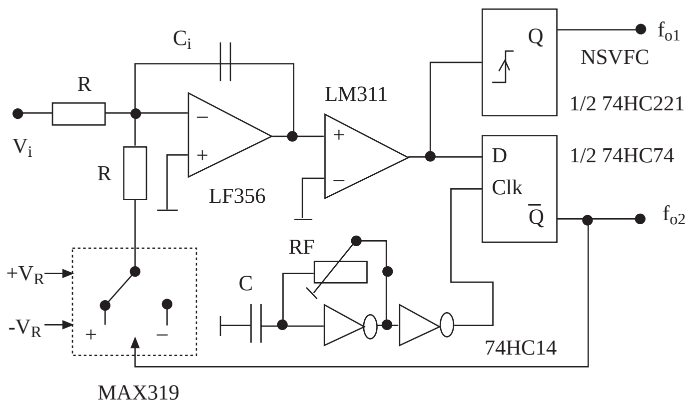

Figure 15. Experimental NSVFC1 simplified circuit diagram.

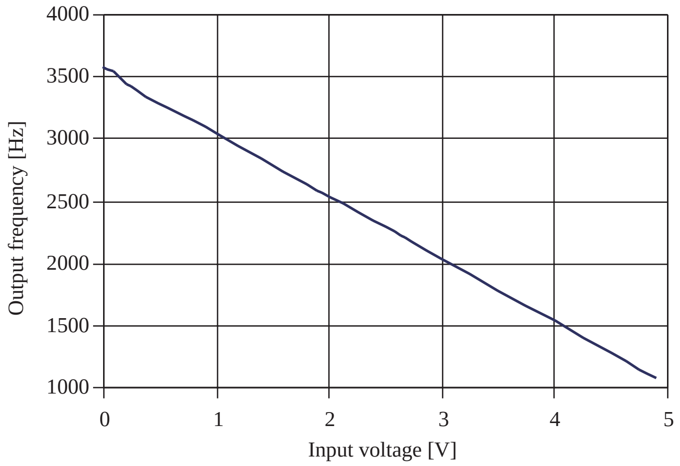

Figure 16. Graph of voltage/frequency characteristic of realized experimental NSVFC1.

Table. Some measured values V_i and f_o of realized experimental NSVFC1.

V_i	0.00	0.10	0.50	1.01	1.20	1.41	1.61	2.01	2.51	3.01	V
f_o	2.84	2.73	2.53	2.28	2.02	2.84	2.73	2.53	2.28	2.02	kHz

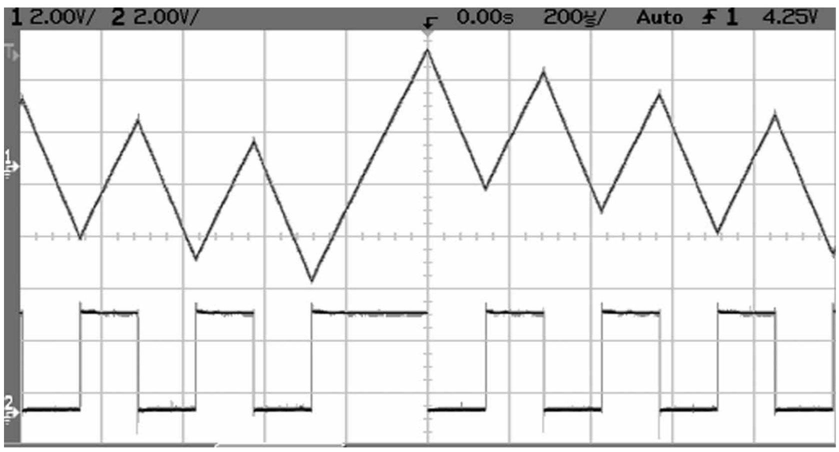

Figure 17. The oscilloscope photograph of the integrator and D-flip flop output of SVFC.

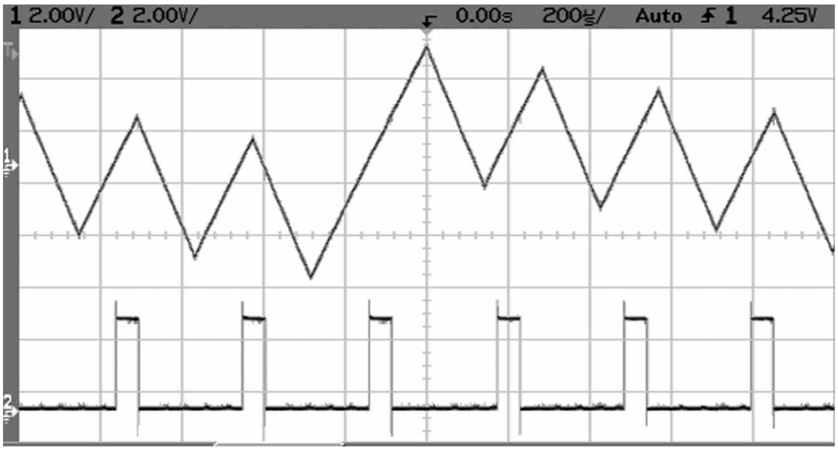

Figure 18. The oscilloscope photograph of the integrator and one shot output of NSVFC1.

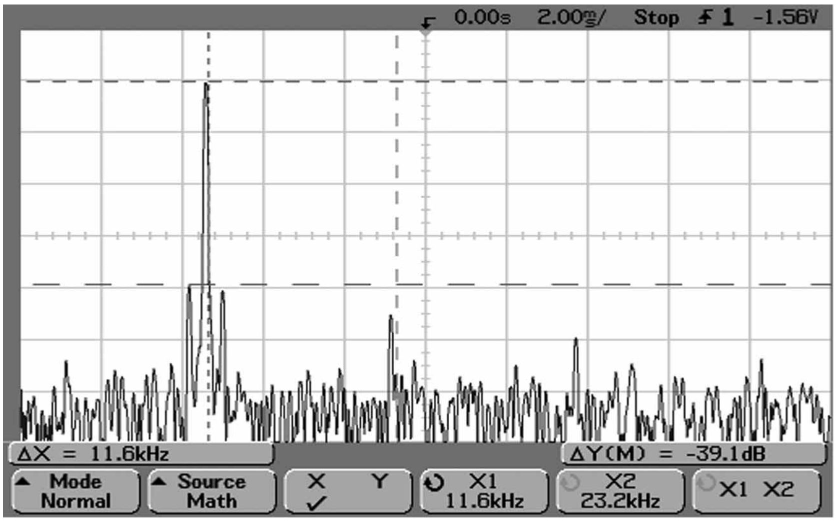

Figure 19. The frequency spectrum of traditional $\Sigma - \Delta V/f$ converter.

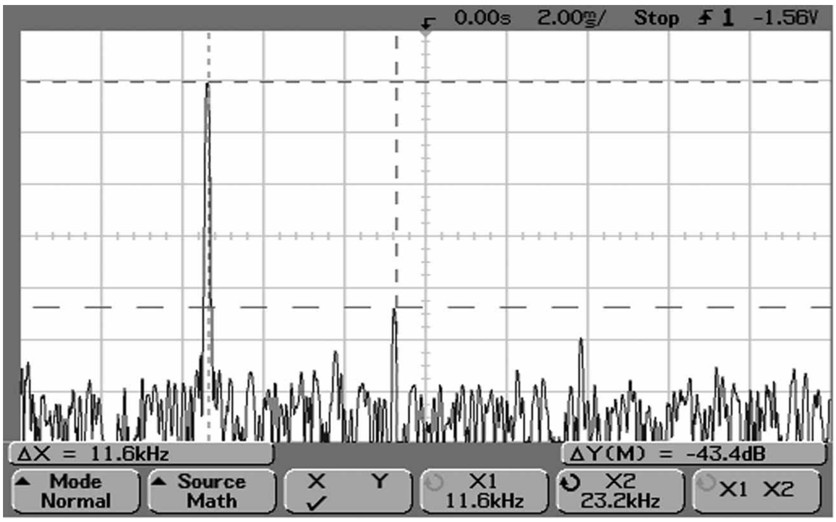

Figure 20. The frequency spectrum of new, modified $\Sigma - \Delta V/f$ converter (NSVFC1).

In Figure 21 the oscilloscope photograph of the integrator and one shot output of NSVFC1 is shown during the error function (missing pulse) for $V_i = 0.032$ V. In NSVFC1 this error is not corrected, but in NSVFC2 is corrected by additional logic.

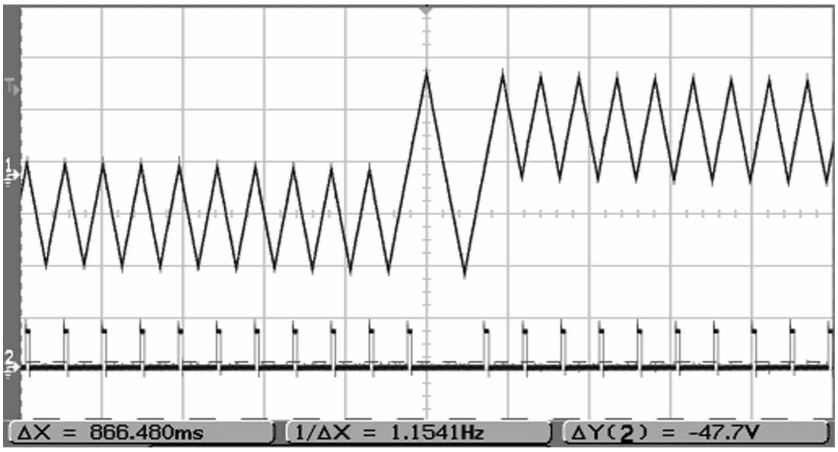

Figure 21. The oscilloscope photograph of the integrator and one shot output of NSVFC1. Error function of the NSVFC1 is shown (missing pulse) for $V_i = 0.032$ V.

7. NSVFC Used in Fractional Phase Locked Loop Frequency Synthesizer

The fractional frequency synthesizer is similar to the divide-by-N phase locked loop (PLL), however, with assistance of the NSVFC, the output frequency of the voltage-controlled oscillator (VCO) is not restricted integral multiples of the reference signal only. Rather, it can also be locked to the fractional multiplies. With NSVFC, fractional frequency synthesizer can be simply realized [13], [14].

The block diagram of experimental fractional PLL synthesizer is shown in Figure 22. If the VCO is locked to the reference frequency, then:

$$f_d = f_r \tag{37}$$

where is f_r reference frequency and f_d is frequency on the output of NSVFC. Because is given by (38):

$$f_d = f_o(1 - V_i/V_R)/2 \tag{38}$$

where f_o is frequency of VCO. After substituting for f_d from (38) into equation (37), frequency of VCO is given by (39):

$$f_o = 2f_r 1/(1 - V_i/V_R) \tag{39}$$

The VCO frequency f_o can be changed according equation (39) by means of changing V_i.

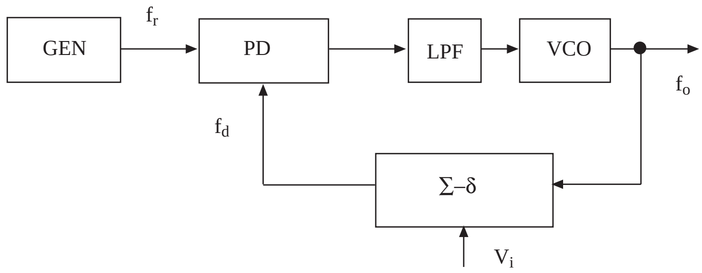

Figure 22. The block diagram of experimental fractional PLL synthesizer, f_r - ref. frequency, f_o - output frequency, V_i - control voltage, GEN - generator, PD - phase detector, LPF-lowpass filter, VCO - voltage controlled oscillator.

8. Conclusion

A very detailed look at the concept of new type sigma-delta voltage to frequency converter circuit has been presented in this article. A prototype system was constructed to verify operation of the converter. Analysis, simulation and prototype of new type voltage to frequency converter were described. The NSVFC simulation results and measured results were compared. From analysis, simulation and measured results can be seen very good agreement from different points of view. It was pointed out that this new converter has better properties than other synchronous types of VFC. This main disadvantage of SVF described above was removed in new type of NSVFC (Figure 2 NSVFC1 and Figure 8 NSVFC2).

Because output pulses are equally spaced in NSVFC (some spurious spectral lines are rejected), this device can be used as fractional divider and building block for phase locked loop frequency synthesizer.

Acknowledgment

This research work has been supported by New Technologies - Research Center in West Bohemian Region LN00 B084 and partly also by Spezial-Electronic (Maxim IC's).

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