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Accurate Prediction of Crosstalk for RC Interconnects

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Abstract

This work proposes an accurate crosstalk noise estimation method in the presence of multiple RC lines for use in design automation tools. The method correctly models the loading effects of non switching aggressors and aggressor tree branches using resistive shielding effect and realistic exponential input waveform. Noise peak and width expressions derived show very good results in comparison to HSPICE results. Results show that average error for noise peak is 4.1% and for the width is 6.8% while allowing for very fast analysis.

Key Words: *Coupling noise, Interconnects, Layout Verification, VLSI circuits.*

1. Introduction

Advancements in lithographic process cause circuits to become more crowded leading to further reduction of distances among interconnects. The interaction caused by parasitic coupling between wires, which is generally known as crosstalk, may cause undesired effects such as positive and negative glitches, overshoot, undershoot, signal delays or even delay reduction. If crosstalk effects on the victim net are large, they can propagate into storage elements that connected to victim line and can cause permanent errors.

Inductance effects in on-chip interconnects becomes increasingly important with smaller rise times and lower wire resistance especially in global interconnects. However for most on-chip lines or interconnects, capacitive effects are still the dominant factor therefore inductance can be safely ignored.

In order to deal with the challenges associated with crosstalk noise, noise estimation and avoidance tools and techniques should be included early into the IC design cycle. Therefore, during signal integrity verification we should confirm that noise pulse width and peak values on sensitive nodes are below the recommended threshold levels, and a given routing solution will not lead to logic failures caused by the coupled noise.

In the past, SPICE-based simulators have been traditionally used to calculate crosstalk noise in signal lines. Due to density of interconnect lines, these simulations are time inefficient. Therefore, a rapid and accurate crosstalk noise estimation alternative is necessary to ensure signal integrity in a limited design cycle time.

Several papers have been published that model crosstalk effects using simple lumped circuit models. Vittal [1] modeled each aggressor and victim net by a simple L-type lumped RC circuit and obtained a bound for crosstalk noise using a step input. Later, extensions to his model are made by [2, 3] to consider a saturated

ramp input or a π -type lumped RC circuit. Cong later proposed a $2-\pi$ model [4] that offered better accuracy than previous models. In this model, the victim line is modeled using the $2-\pi$ model while aggressor net is simplified as a saturated ramp at the coupling node. In the model, the distributed aggressor net characteristics and its driver information have been included into the ramp slew rate at the coupling location. Obviously, this method requires some sort of pre-processing on the aggressor line. Later, modifications are made to this model and an improved $4-\pi$ model has been proposed [5]. In this improved version, the model is extended to include the aggressor distributed line characteristics. However, the approach uses decoupling, and during the decoupling it ignores victim loading effect on aggressor coupling node.

This work extends the approach in [5] and, based on the $4-\pi$ model, it introduces a new multi-line model that considers non-switching aggressors as well as switching aggressors. The realistic exponential waveforms are considered during victim noise derivations. Being different from previous $4-\pi$ model, the passive aggressors are represented as equivalent capacitances to the victim line rather than simple lumped coupling capacitance. Equivalent capacitances represent the loading effect of passive aggressors on victim line and have been formulated by including realistic exponential aggressor waveform and resistive shielding. Similarly, the tree branches are also formulated by an equivalent capacitance.

The previous methods concentrate mostly on saturated ramp or step inputs for aggressors. It has been argued in [6–8] that active aggressors are more closely approximated by exponential waveforms. Therefore, an exponential type aggressor waveform has been utilized in the derivations.

Based on the model, first aggressor coupling node waveform is derived. Then, after calculating the transfer function between aggressor coupling node and victim receiver, victim noise waveform has been derived. Noise peak and width are the two parameters to determine whether the noise is acceptable. Therefore, the closed form analytic expressions for peak noise and noise width are also formulated. The results for 1000 random test circuits are compared against HSPICE simulations. Simulations are also done for multiple switching aggressors and results show good agreement to HSPICE results.

The remain of this paper is organized as follows. Section 2 explains the $4-\pi$ model template. In Section 3, the equivalent capacitance formula for passive aggressors and for victim line has been derived. RC trees and branching is discussed in Section 4.

For noise formulation, aggressor coupling voltage is first calculated in Section 5 noting victim loading and any possible aggressor tree branches. Finally, in Section 6, output voltage is formulated and the proposed complete crosstalk model is explained in detail. Closed form expressions for noise peak and width are formulated. The model has been tested extensively using 1000 randomly generated circuits and verified using HSPICE. The results are shown in Section 7 in tabular form. Section 8 deals with multiple aggressor case. A comparison is made between the proposed model and the previous method [5] and results are shown along with HSPICE results.

2. The $4-\pi$ Model

The multiline model will be developed based on $4-\pi$ model parameters. In the $4-\pi$ model, both victim and the aggressor net are modeled using the $2-\pi$ circuits [5]. Finally, we obtain the following template circuit, shown in Figure 1. In this model, effective resistances R_d and R_{th} model the victim and aggressor drivers, respectively. Drivers are represented by linear resistors using the method described in [9]. Other RC parameters are calculated based on technology and the geometric information from Figure 1a. The coupling node (node 2)

is set to be the center of the coupling portion of the victim net.

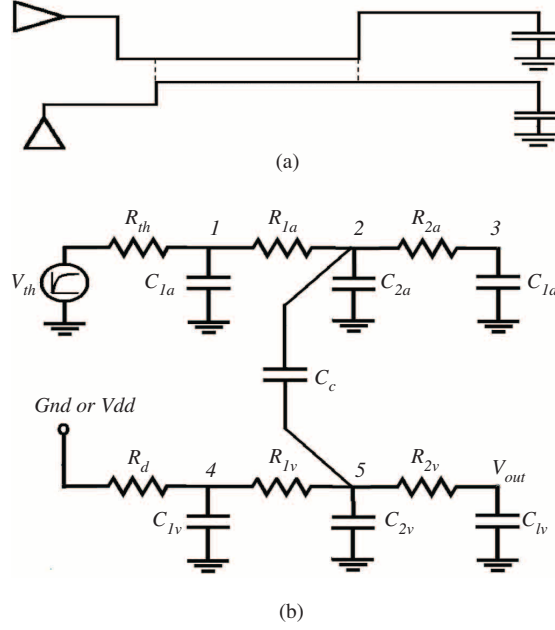


Figure 1. The $4-\pi$ model for two coupled interconnects.

We assume the upstream and downstream resistance/ capacitance at node 2 be R_{1a}/C_{ua} and R_{2a}/C_{da} , respectively. Similarly for victim net, let's assume upstream and downstream resistance/capacitance at node 5 to be R_{1v}/C_{uv} and R_{2v}/C_{dv} respectively. Then, for aggressor and the victim, we have:

$$C_{1a} = C_{ua}/2, \quad C_{2a} = (C_{ua} + C_{da})/2 \text{ and, } C_{la} = C_{da}/2 + C_{lda}$$

$$C_{1v} = C_{uv}/2, \quad C_{2v} = (C_{uv} + C_{dv})/2 \text{ and, } C_{lv} = C_{dv}/2 + C_{ldv}$$

Here, C_{lda} and C_{ldv} represent the load capacitances for aggressor and victim lines, respectively.

3. Passive Aggressor Modeling By An Equivalent Capacitance

A victim can be coupled to many non-switching (passive) aggressors. Previously the loading effect of a passive aggressor is simply taken as a coupling capacitor at victim coupling point [4], [5]. However, a passive aggressor follows victim waveform and contributes to the stability of the victim line. Therefore, equivalent load capacitance at the victim coupling point is less than coupling capacitance and can be formulated using coupling/branching admittance concept [10]. In this paper, equivalent capacitance formula for a passive aggressor is derived assuming an exponential aggressor waveform. For this, the passive aggressor is first reduced to the simple circuit shown in Figure 2b, where:

$$R'_a = R_{th} + R_{1a} \quad (1)$$

$$C'_a = C_{2a} + C_{la} + (R_{th}^2 / (R_{th} + R_{1a})^2) C_{1a} \quad (2)$$

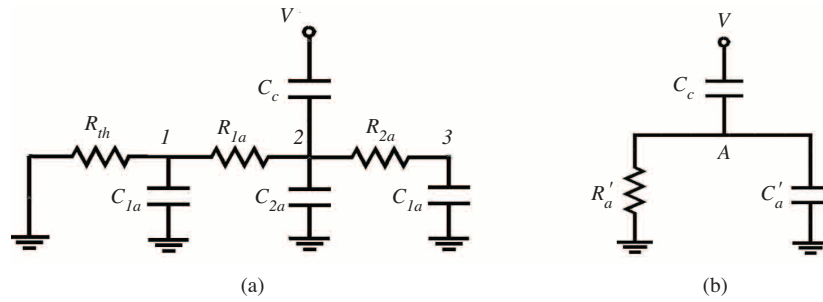


Figure 2. A non-switching aggressor net coupled to the victim line.

Then, for matching purposes, the victim waveform is assumed to be a normalized exponential voltage, as shown in Figure 3. The equivalent capacitance for the passive aggressor can now be formulated. The currents coming from victim node should be same both cases:

$$I = C_c \left[\frac{dV_V(t)}{dt} - \frac{dV_A(t)}{dt} \right] = C_{eq} \frac{dV_V(t)}{dt} \quad (3)$$

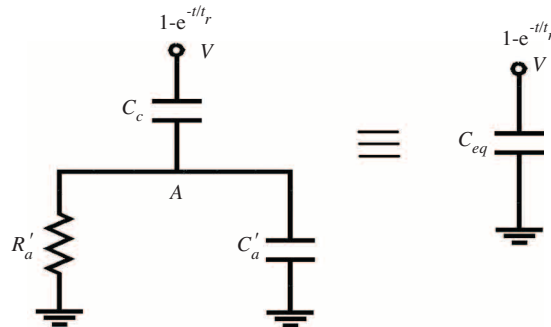


Figure 3. Passive Aggressor line reduction.

Assuming zero initial condition and exponential waveform, we can calculate the equivalent capacitance by integrating (3) over $0 \leq t \leq 5t_r$ interval (t_r is the exponential rise time constant):

$$C_{eq} = C_c [1 - V_A(5t_r)] \quad (4)$$

Now, considering left part of Figure 3,

$$C_c \left[\frac{dV_V(t)}{dt} \right] = (C_c + C'_a) \frac{dV_A(t)}{dt} + \frac{V_A(t)}{R'_a} \quad (5)$$

$$V_A(t) = \frac{C_c R'_a}{t_r - R'_a (C_c + C'_a)} \left[e^{-\frac{t}{t_r}} - e^{\frac{-t}{R'_a (C_c + C'_a)}} \right] \quad (6)$$

Inserting $V_A(5t_r)$ in (4), C_{eq} formula is given as:

$$C_{eq} = C_c \left[1 + \frac{C_c R'_a}{t_r - R'_a (C'_a + C_c)} \cdot e^{\frac{-5t_r}{R'_a (C'_a + C_c)}} \right]. \quad (7)$$

A passive aggressor coupled to the victim line can be reduced to an equivalent capacitor using the formula derived above and this capacitor would then be taken in parallel with C_{2v} at node 5. Finally, the circuit would reduce to the one in Figure 1.

4. RC Trees and Branch Modeling

Previous work in [5] treats aggressor net branches simply as lumped capacitances at the branching point. However, the capacitance seen at the branching node is less than the total branch capacitance due to resistive shielding effect. Hence, the approach in [5] is incorrect. Here, an equivalent capacitance formula for tree branches is derived noting the exponential aggressor waveform.

First tree branches are reduced to a simple π model following the moment matching method as demonstrated in [10]. Then, this model reduces to an equivalent branching capacitance C_{eq-br} (Figure 4) considering an exponential waveform on input node A.

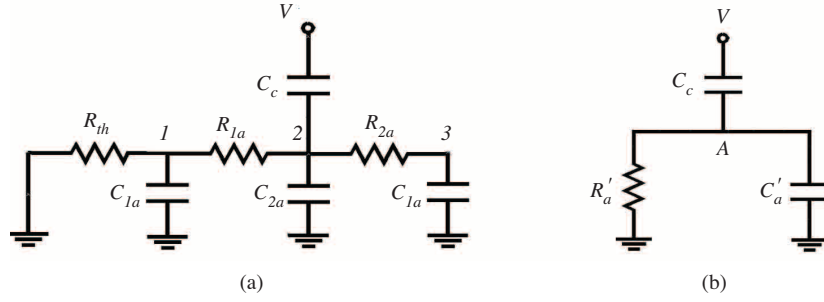


Figure 4. Obtaining an equivalent branching capacitance.

In Figure 4, we can equate the currents on node A for both circuits:

$$C_{eq-br} \frac{dV_A(t)}{dt} = C_a \frac{dV_a(t)}{dt} + C_b \frac{dV(t)}{dt} \quad (8)$$

Assuming a rising exponential voltage on input node and zero initial condition, we can obtain an equivalent branching capacitance after integrating both sides of above equation over $0 \leq t \leq 5t_r$ time interval:

$$C_{eq-br} = C_a + C_b V_B(5t_r) \quad (9)$$

Then by applying KCL on node B, one obtains the relation

$$\frac{dV_B(t)}{dt} + \frac{V_B(t)}{RC_b} = \frac{1 - e^{-t/t_r}}{RC_b} \quad (10)$$

Upon solving the differential equation and inserting $t = 5t_r$

$$V_B(5t_r) = 1 + \frac{RC_b}{t_r - RC_b} \cdot e^{-5t_r/RC_b} \quad (11)$$

Finally, this value can be inserted in (9), giving

$$C_{eq-br} = C_a + C_b \left[1 + \frac{RC_b}{t_r - RC_b} \cdot e^{-5t_r/RC_b} \right] \quad (12)$$

5. Aggressor Waveform Calculation at Coupling Node

Proposed model uses a reduced transfer function between aggressor coupling node and the victim node, hence results in small accuracy loss compared to the method in [5]. In previous work, the direct transfer function between aggressor input and victim output is first calculated, then dominant pole approximation is hired over the whole transfer function to reduce complexity. However, too much use of dominant pole approximation always reduces model accuracy.

In the proposed model, the aggressor waveform at the coupling node is first calculated and then entered to the transfer function between the coupling node and the victim output to obtain victim noise voltage. Compared to [5], the dominant pole approximation is used moderately which results in increased accuracy.

In order to model the coupling node aggressor waveform correctly, victim-loading effect on the aggressor node needs to be calculated. The loading effect is smaller than the coupling capacitor due to resistive shielding. The victim line can be reduced into an equivalent capacitor C_{eqv} using the quiet aggressor/victim net reduction techniques which was summarized in Section 3.

The aggressor branches after the coupling point are also reduced to an equivalent capacitance C_{req} using the tree branch reduction techniques given earlier. Here, we consider the right part of the aggressor net after the coupling point which is a π -type circuit (Figure 5).

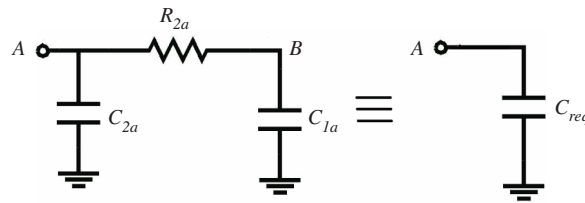


Figure 5. Tree branch reduction on right part of aggressor net.

The equivalent branching capacitance C_{req} is similarly given by (shown here for convenience) the relation

$$C_{req} = C_{2a} + C_{1a} \left[1 + \frac{R_{2a}C_{1a}}{t_r - R_{2a}C_{1a}} e^{\frac{-5t_r}{R_{2a}C_{1a}}} \right]. \quad (13)$$

After application of the reduction techniques, the 4- π network, shown in Figure 1b, reduces to Figure 6 for aggressor coupling node voltage calculation.

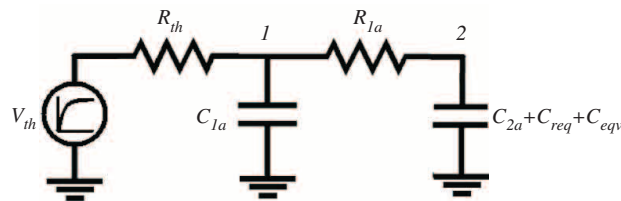


Figure 6. The circuit for aggressor waveform calculation at coupling node.

From Figure 6,

$$V_1(s) = \frac{Z}{R_{th} + Z} V_{in}(s), \quad (14)$$

where,

$$\frac{1}{Z} = \frac{1}{R_{1a} + \frac{1}{sC}} + sC_{1a} \quad (15)$$

and,

$$C = C_{2a} + C_{req} + C_{eqv} :$$

then we have

$$V_2(s) = \frac{1}{sCR_{1a} + 1} V_1(s). \quad (16)$$

Finally, the transfer function between the input and coupling node 2 is:

$$\frac{V_2(s)}{V_{in}(s)} = \frac{1}{st_a + 1}, \quad (17)$$

where

$$t_a = C_{1a}R_{th} + (C_{2a} + C_{veff} + C_{reff})(R_{th} + R_{1a}).$$

We note that t_a is, in fact, the Elmore delay between the input and Node 2. For unit saturated exponential input $V_{in}(t) = 1 - e^{-t/t_r}$, we obtain:

$$V_2(t) = 1 + \frac{1}{t_r - t_a} (t_a e^{-t/t_a} - t_r e^{-t/t_r}). \quad (18)$$

This waveform, when plotted, represents a delayed exponential waveform as expected. However, it contains two exponential terms, and should be reduced to only one term for simplicity. If we assume the delayed waveform at coupling node to be

$$V_2(t) = 1 - e^{-t/t_x}. \quad (19)$$

We equate these two waveforms:

$$1 + \frac{t_a}{t_r - t_a} e^{-t/t_a} - \frac{t_r}{t_r - t_a} e^{-t/t_r} = 1 - e^{-t/t_x}.$$

The area under both exponential functions should be same:

$$\int_0^{\infty} \frac{t_a}{t_r - t_a} e^{-t/t_a} - \int_0^{\infty} \frac{t_r}{t_r - t_a} e^{-t/t_r} = \int_0^{\infty} -e^{-t/t_x}.$$

It turns out that

$$t_x = t_r + t_a. \quad (20)$$

The new rising exponential time constant t_x calculated has been verified by plotting the function in (19) simultaneously with HSPICE result. The following parameter values were used for the verification: $R_{th}=200 \Omega$, $R_{1a} = R_{2a} = 120 \Omega$, $R_d=250 \Omega$, $R_{1v} = R_{2v} = 100 \Omega$. The coupling capacitance C_c is taken as 150 fF. Other capacitances are given as follows: $C_{ua} = C_{da} = 100\text{fF}$, $C_{uv} = C_{dv} = 100 \text{ fF}$. Let load capacitances for aggressor and victim line be 50 fF each. Also a normalized aggressor voltage is assumed and aggressor rise time t_r is chosen as 150 ps.

Figure 7 shows the calculated waveform (19) vs. the result from HSpice at aggressor coupling node. Although there is some mismatch, especially before the waveform saturates, the time corresponding to the 50% point shows good matching. For the given parameter values above, the model predicts the new rise time constant (t_x) as 305 ps while HSpice calculates it as 314 ps. The model error is only 2.8%. For 100 random circuits, the model has been verified and error corresponding to each case is calculated and it has been found the absolute error value remains less than 3.5%.

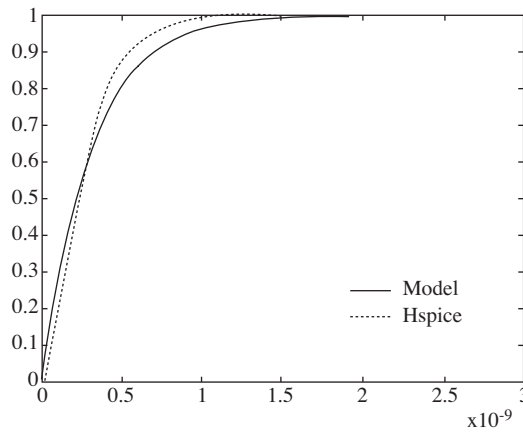


Figure 7. Coupling point waveform of the aggressor.

6. Output Voltage Formulation

In the previous section, the aggressor waveform at the coupling node is formulated by considering the exponential aggressor input. Now, the aggressor waveform at coupling location needs to be entered to the transfer function to calculate noise as shown in Figure 8.

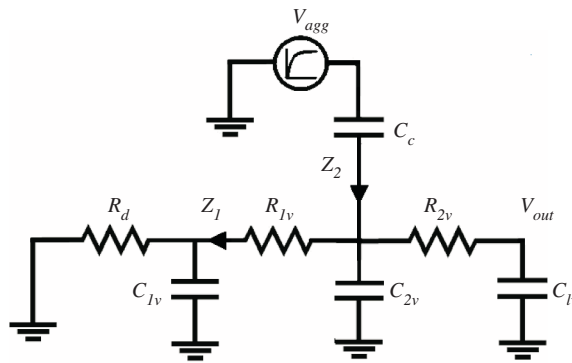


Figure 8. Output voltage calculation.

Referring to Figure 8, we have,

$$\frac{1}{Z_1} = \frac{1}{R_d} + sC_{1v}, \tag{21}$$

$$\frac{1}{Z_2} = \frac{1}{R_{2v} + sC_{lv}} + sC_{2v} + \frac{1}{Z_1 + R_{1v}}, \tag{22}$$

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_c}} V_{agg}(s), \quad (23)$$

$$V_{noise}(s) = \frac{1}{sC_{l_v} R_{2v} + 1} V_2(s). \quad (24)$$

After substituting (23) in $V_{noise}(s)$ equation in (24), Dominant-Pole approximation method [4, 11, 12] is used to reduce complexity of the transfer function. Finally, we have:

$$\frac{V_{noise}(s)}{V_{agg}(s)} = \frac{s\tau_x}{\tau_v s + 1} \quad (25)$$

where,

$$\tau_v = R_d(C_c + C_{1v} + C_{2v} + C_{lv}) + R_{1v}(C_c + C_{2v} + C_{lv}) + R_{2v}C_{lv}$$

and

$$\tau_x = (R_d + R_{1v})C_c.$$

If we insert the exponential function in (18) as the aggressor input voltage, we obtain the following noise waveform:

$$V_{noise}(t) = \frac{\tau_x}{t_x - \tau_v} \cdot (e^{-t/t_x} - e^{-t/\tau_v}). \quad (26)$$

By differentiating $V_{noise}(t)$ with respect to t , the time the voltage peaks t_{peak} can be found:

$$t_{peak} = \frac{t_x \tau_v}{t_x - \tau_v} \log_n(t_x / \tau_v). \quad (27)$$

The noise peak voltage V_{peak} is found after inserting (27) in (26):

$$V_{peak} = \frac{\tau_x}{\tau_v - t_x} \left[(t_x / \tau_v)^{\frac{t_x}{\tau_v - t_x}} - (t_x / \tau_v)^{\frac{\tau_v}{\tau_v - t_x}} \right] \quad (28)$$

Noise peak has been traditionally used as a metric to determine if the noise is at an acceptable level. However, the noise width is also necessary in determining whether a noise pulse can go through a receiver. If noise peak exceeds the threshold, but does not carry sufficient width, the noise may not be received at the receiver output at all. Therefore, noise width should be considered.

The noise peak expression was already derived in (27). For noise width, the threshold is usually taken as 50% of V_{peak} . Considering equation (26) and the threshold, one can obtain a function $f(t)$ which can be used in Newton's iteration method to solve for the t_1 and t_2 time instances:

$$\frac{\tau_x}{\tau_v - t_x} \cdot (e^{-t/\tau_v} - e^{-t/t_x}) = \frac{\tau_x}{2(\tau_v - t_x)} \left[(t_x / \tau_v)^{\frac{t_x}{\tau_v - t_x}} - (t_x / \tau_v)^{\frac{\tau_v}{\tau_v - t_x}} \right] \quad (29)$$

where,

$$f(t) = e^{-t/\tau_v} - e^{-t/t_x} - 0.5(t_x / \tau_v)^{t_x / \tau_v - t_x} + 0.5(t_x / \tau_v)^{\tau_v / \tau_v - t_x} = 0$$

and

$$f'(t) = e^{-t/\tau_v} / \tau_v - e^{-t/t_x} / t_x.$$

This method converges very rapidly if the initial guesses are taken carefully. The initial guesses of t_1 and t_2 are taken as $1/4 t_{peak}$ and $4t_{peak}$ respectively. The values of t_1 and t_2 are updated using the iteration formula given below:

$$t_{1_{k+1}} = t_{1_k} - \frac{f(t_{1_k})}{f'(t_{1_k})} \text{ and } t_{2_{k+1}} = t_{2_k} - \frac{f(t_{2_k})}{f'(t_{2_k})}. \quad (30)$$

Then, the noise width is defined by

$$t_{width} = t_2 - t_1. \quad (31)$$

The algorithm converges rapidly after only a few iterations.

Model Summary:

The following steps summarize for the proposed model:

1. For each passive aggressor, calculate the equivalent capacitance value C_{eq-a} at victim coupling point. This capacitor is then placed in parallel at victim line coupling point.
2. Repeat the same procedure in step (a) for the victim line, and find the equivalent capacitance of the victim line C_{eq-v} . This capacitor updates the value of C_{2a} at the active aggressor coupling point. The formula for C_{eq-v} is slight variation of equation (7).
3. Any aggressor tree branches are also reduced to an equivalent branching capacitance C_{eq-br} at branching point.
4. Calculate the aggressor coupling node waveform. Find the new rise time constant t_x of the exponential waveform.
5. Calculate other time constants τ_x , and τ_v .
6. Obtain noise peak value V_{peak} and the time it occurs, which is t_{peak} .
7. Use $t_{peak}/4$ and $4t_{peak}$ as initial guesses in the iteration formula derived for the width, and calculate the corresponding time instances t_1 and t_2 values to determine the noise pulse width, namely t_{width} by (31).

7. Validation of the Proposed Model

The model has been tested extensively and its accuracy has been compared against SPICE simulation results. 1000 random test circuits having 6-node template circuit topology have been generated to simulate real world cases using 0.13-micron parameters. The parameter ranges were taken as follows [5]: R_d and R_{th} are 10–1500 Ohms; load capacitances for victim and aggressor lines are 5–50 fF; aggressor and victim wire resistances are 10–250 Ohms; and finally t_r is chosen in the range between 20–500 ps.

Table 1. The percentage of nets that fall into the error ranges.

Error Range	V_{peak}	t_{width}
Within $\pm 5\%$	87.4%	74.9%
Within $\pm 10\%$	97.9%	86.3%
Within $\pm 15\%$	99.3%	93.1%
Avg. Error	4.1%	6.8%

Table 1 shows the percentage of nets that fall into different error ranges. For example, 97.9% of nets have errors less than 10 percent when predicting the noise peak voltage. Results show an average error of 4.1% for the noise peak and an average error of 6.8% for the noise width.

Table 2. Experimental results obtained for industrial circuits.

Case #	Act/Total	Noise Peak (Hspice)mV	(Becer) mV	err %	(Model) mV	err %	Noise width (Hspice)nS	(Becer) nS	Err %	(Model) nS	err %
1	2 / 2	252	219	13.09	258	2.38	1.28	1.46	14.06	1.33	3.91
2	3 / 5	340	315	7.35	354	4.12	1.46	1.57	7.53	1.38	5.48
3	3 / 5	384	345	10.15	391	1.82	1.29	1.37	6.20	1.35	4.65
4	3 / 5	390	358	8.21	371	4.87	1.58	1.71	8.23	1.44	8.86
5	4 / 5	492	438	10.98	470	4.47	1.64	1.80	9.76	1.51	7.93
6	3 / 3	331	305	7.85	354	6.95	1.47	1.66	12.93	1.46	0.68
7	2 / 3	220	197	10.45	203	7.73	1.18	1.29	9.32	1.24	5.08
8	2 / 2	296	259	12.50	272	8.11	1.12	1.28	14.28	1.21	8.04
9	5 / 6	394	364	7.61	384	2.54	1.19	1.41	18.48	1.26	5.88
10	4 / 5	125	108	13.60	118	5.60	2.01	2.23	10.94	1.85	7.96
11	6 / 6	470	417	11.28	453	3.62	1.71	1.88	9.94	1.82	6.43
12	6 / 6	360	314	12.78	383	6.39	1.66	1.85	11.45	1.77	6.63
13	8 / 8	510	449	11.96	532	4.31	1.59	1.77	11.32	1.47	7.55
14	5 / 8	490	447	8.78	477	2.65	1.09	1.17	7.34	0.99	9.17
15	4 / 4	526	468	11.03	512	2.66	1.89	2.01	6.35	2.03	7.41
16	3 / 3	183	169	7.65	177	3.28	0.95	1.15	21.05	0.83	12.63
17	4 / 4	372	344	7.53	383	2.96	1.13	1.25	10.62	1.01	10.62
18	2 / 2	417	365	12.47	402	3.60	1.38	1.54	11.59	1.41	2.17
19	7 / 8	517	440	14.89	477	7.74	1.44	1.61	11.81	1.38	4.17
20	6 / 8	550	478	13.09	588	6.91	2.38	2.54	6.72	2.43	2.1
21	5 / 8	523	479	8.41	539	3.06	1.79	1.93	7.82	1.72	3.91
22	4 / 7	411	365	11.19	393	4.38	2.14	2.41	12.61	2.28	6.54
23	5 / 6	464	419	9.70	433	6.68	0.87	0.98	13.79	0.79	9.2
24	4 / 5	412	369	10.44	388	5.83	1.24	1.39	12.10	1.13	8.87
25	6 / 6	510	465	8.82	481	5.69	1.34	1.53	14.18	1.22	8.96
26	3 / 4	282	249	11.70	269	4.61	0.79	0.91	15.19	0.69	12.66
27	4 / 5	324	289	10.80	314	3.09	1.55	1.74	12.26	1.41	9.03
28	5 / 5	482	441	8.51	452	6.22	1.01	1.24	19.80	0.96	4.95
29	3 / 3	212	171	19.34	227	7.08	0.89	1.05	17.97	0.78	12.36
30	5 / 6	395	361	8.61	389	1.52	2.12	2.33	9.91	1.96	7.55
Average Error				10.7%		4.7%			11.9%		7.05%

8. Multiple Active Aggressors

In a real circuit, a given victim line can be coupled to many switching (active) aggressors. In this case, Superposition theorem can be hired to calculate the total cross-coupling noise. With Superposition, each active aggressor is switched one at a time while holding other aggressor drivers quiet. The noise contributions are summed at the end to calculate total noise at the victim end.

If there are N switching aggressors, it is necessary to calculate noise N times to obtain final result, hence time complexity is linear. Prior to any noise calculation, an equivalent capacitance value should be calculated for each aggressor using (7). The equivalent capacitance values are utilized during Superposition to represent non-switching aggressors and this reduces the complex multiline network into a manageable $4\text{-}\pi$ template shown in Figure 1 during each Superposition step.

To validate our results, the design data for a real microprocessor design in $0.13\ \mu\text{m}$ technology [5] have been used and 30 noise-prone nets have been obtained. Table II shows experimental results obtained for multiple

aggressor case. Various interconnect length, width and spacing are examined. Interconnect lengths varied from 100 μm up to 2 mm. Some of these nets also included some tree branches.

Experiments are performed up to eight aggressors. The second column in the table specifies the number of switching aggressors and the total number of aggressors. In these experiments, different switching windows of aggressors have also been considered.

In Table 2, noise peak and width values of the previous approach in [5], and the proposed approach have been compared with HSPICE results. HSPICE simulation utilized a $20\text{-}\pi$ representation for each interconnect line along with distributed coupling capacitance. The proposed approach has an average error of only 4.7% for the noise peak, and 7.1% for the noise width. In comparison, Becer's approach [5] has an average error of 10.7% for the noise peak, and 11.9% for the noise width. The inclusion of victim loading effect, the equivalent capacitance representation for passive aggressors and moderate use of dominant pole approximation makes our proposed model superior in terms of accuracy. On the other hand, the CPU time for these 30 industrial nets ranges from 0.02 mS to 0.15 mS on a 3.0 GHz Pentium IV machine.

9. Conclusion

This paper proposed an accurate method to estimate crosstalk noise in the presence of multiple aggressor lines. The proposed model presented a complete multilayer noise model by representing active and passive aggressors simultaneously. For passive aggressors, an equivalent capacitance model has been derived noting realistic exponential aggressor waveform and formulation included resistive shielding effects. General closed-form expressions for cross-talk noise peak and width have been developed. Closed form expressions for noise width and height are compared against HSPICE and results are very encouraging. Results show that the average error for noise peak is 4.1% and for the width is 6.8% while allowing for very fast analysis. The model has also been verified for multi aggressor scenario. The proposed model can be used to allow time-efficient accurate analysis of multi conductor line structures.

References

- [1] A. Vittal and M. Marek-Sadowska. "Crosstalk reduction for VLSI", *IEEE Transactions on Computer-Aided Design*, Vol. 16, pp. 1817-24, 1997.
- [2] A. B. Kahng, S. Muddu, and D. Vidhani, "Noise and delay uncertainty studies for coupled RC interconnections", *IEEE Int. ASIC/SOC Conf.*, pp. 3-8, 1999.
- [3] S. Nakagawa, D. M. Sylvester, J. McBride, and S.-Y. Oh "On-chip crosstalk noise model for deep submicrometer ULSI interconnect", *H. P. Journal*, Vol. 49, pp.39-45, 1998.
- [4] J. Cong, D.Z. Pan, and P. V. Srinavas, "Improved crosstalk modeling for noise constrained interconnect optimization", *Proceedings of ASP/DAC*, pp. 373-378, 2001.
- [5] M. R. Becer, D. Blaauw, V. Zolotov, R. Panda, I. N. Hajj, "Analysis of noise avoidance techniques in DSM interconnects using a complete crosstalk noise model", *2002 Design, Automation and Test in Europe Conference*, pp. 456-464, 2002.

- [6] T. Sato, Y. Cao, K. Agarwal, D. Sylvester, and C. Hu, "Bidirectional closed-form transformation between on-chip coupling noise waveforms and interconnect delay change curves," *IEEE Transactions on Computer-Aided Design*, vol. 22, no. 5, pp. 560-572, 2003.
- [7] K. Agarwal, Y. Cao, T. Sato, D. Sylvester, and C. Hu, "Efficient generation of delay change curves for noise-aware static timing analysis" *Proc. of Asia and South Pac. Design Automation Conf.*, pp. 77-84, 2002.
- [8] M. Kuhlmann, S. S. Sapatnekar, K. K. Parhi, "Efficient crosstalk estimation", *International Conference on Computer Design (ICCD '99)*, pp. 266 – 272, 1999.
- [9] R. Levy, D. Blaauw, G. Braca, A. Dasgupta, A. Grinshpon, C. Oh, B. Orshav, S. Sirichotiyakul, and V. Zolotov, "Clarinet: A noise analysis tool for deep submicron design", in *Proc. Int. Conf. Computer-Aided Design*, Nov. 2002, pp. 587-594.
- [10] J. Qian, S. Pulella, and L. T. Pillage, "Modeling the effective capacitance for the RC interconnect of CMOS gates," *IEEE Transactions on Computer-Aided Design*, Vol. 13, pp. 1526–1535, 1994.
- [11] L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis", *IEEE Transactions on Computer-Aided Design*, Vol. 9, No. 4, pp. 352 - 366, 1990.
- [12] E. Acar, A. Odabasioglu, M. Celik, and L. Pileggi. "S2p: a stable 2- pole RC delay and coupling noise metric IC interconnects", *Proceedings 9th Great Lakes Symposium on VLSI*, pp 60-63, 1999.