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VLSI-cell placement technique for Architecture of Field Programmable Gate Array (FPGA) design

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Abstract

The Field Programmable Gate Array (FPGA) is an on field programmable device which can be designed for different applications. Various types of software are available for its synthesis. The cell placement depends upon the designing and programming languages used for FPGA. In this paper cell placement technique of FPGA architecture is analyzed for the application of Space Vector Pulse Width Modulation (SVPWM) technique used in speed control of an induction motor. The modulation pulses are produced due to the various components activated and their interconnection in Configurable Logic Blocks (CLBs). Few of its components are so analyzed to find out the reason for their desired output response. This survey has also been conducted to find the correlation of LUTs and formulation of output.

Key Words: *Field Programmable Gate Array (FPGA), Space Vector Pulse Width Modulation (SVPWM), Configurable Logic Blocks (CLBs), Look Up Table (LUT), Routing, Insulated Gate Bipolar Transistor (IGBT).*

1. Introduction

A Field Programmable Gate Array (FPGA) chip often contains tens of thousands of logic blocks with programmable routing channels for custom hardware programming to realize desirable functionality. Normally two Input/ Output (I/O) buffer pads fit into the height of one row and width of one column of one configurable logic blocks (CLBs). The routing channels have the same width for same number of wires, as shown in Figure 1. The FPGA logic blocks is a constitution of 4-input look-up-table (LUT), a multiplexer and a flip-flop connected with a clock which is assumed completely routed through global grid network, as shown in Figure 2.

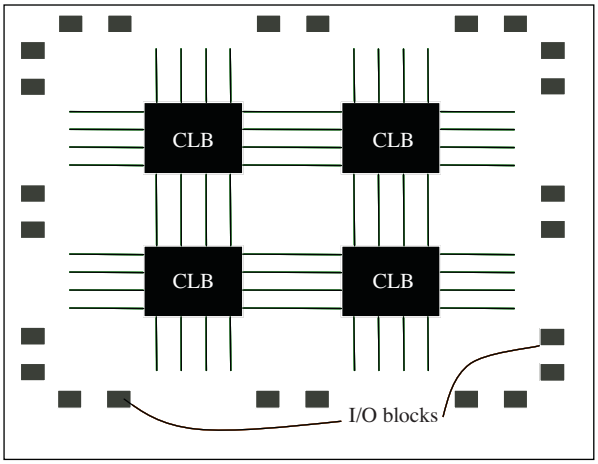

Figure 1. Cross-section of FPGA.

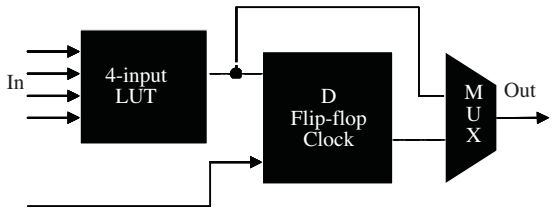

Figure 2. Internal structure of FPGA.

The programming of interconnects is accomplished by the programming of Random Access Memory (RAM) cells whose output terminals are connected to the gates of MOS (Metal Oxide Semiconductor) pass transistors. In this way signal routing between the CLB and the I/O blocks is accomplished by setting the configurable switch matrices accordingly. The complexity of FPGA chip typically depends upon the number of CLBs, which thereby increase the gate count. The clock frequency range is from a few hundred Hz to MHz. It is stated that the dedicated computer-aided tools can increase gate utilization up to 90% [1].

The array of logic blocks can be programmed electrically to realize different designs. In our study we have incorporated space vector pulse width modulation (SVPWM) technique to attain variable speed in induction motor. A cascaded hardware design of very large scale integration (VLSI) and Power Electronics has been constructed. It has been fabricated using Insulated Gate Bipolar Transistor (IGBT) number CT60AM18F. An inverted output DC to three phase AC has been observed and Voltage/Frequency (V/f) speed control technique has been implemented. To accumulate the advantage of wide frequency range of FPGA architecture, it is constructed using the VHDL language. The results of synthesis designing have been discussed and truth table of different types of CLBs has been analyzed.

This paper is formulated under various sections. Section II includes experimental definition and procedure, Section III includes cell placement technique, Section IV includes results & discussion, conclusion and the scope for future work is discussed in Section V.

2. Experimental definition and procedure

The field oriented vector technique is the most compatible and widely used technique for speed control of induction motor for industrial purpose. The SVPWM with its advantages like low energy consumption, improved transient response with less generated noises, less harmonics etc., has been adopted [2, 3].

a. Experimental Setup. IGBT inverter provides rectified power from a single phase AC source. The Xilinx compatible FPGA is used as control unit of IGBT power circuit to implement V/f speed control techniques for the Induction motor. FPGA is generating the control pulses to sustain three phase sine waves 120° apart on which AC induction motor thrives, as shown in Figure 3.

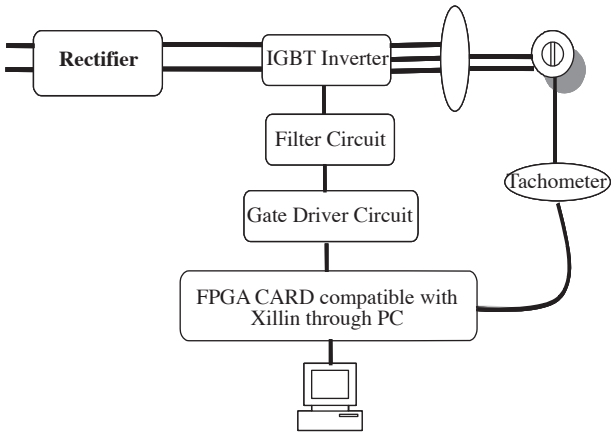

Figure 3. Block Diagram of experimental Setup for VSI controller through FPGA.

b. Circuit Algorithm Involved. There are eight possible combinations of switching states which derive output line-to-line and phase voltages in terms of DC supply voltage. Six of them lead to non-zero phase voltages and two interchangeable states lead to zero phase voltages, as shown in Table 1.

Table 1.

R	Y	B	V_{RN}	V_{YN}	V_{BN}	V_{RY}	V_{YB}	V_{BR}	M	Ang.
0	0	0	0	0	0	0	0	0	0	0
0	0	1	-1/3	-1/3	?	0	-1	1	1	-120^0
0	1	0	-1/3	2/3	-1/3	-1	1	0	1	120^0
0	1	1	-?	1/3	1/3	-1	0	1	1	180
1	0	0	2/3	-1/3	-1/3	1	0	-1	1	0
1	0	1	1/3	-2/3	1/3	1	-1	0	1	-60^0
1	1	0	1/3	1/3	-2/3	0	1	-1	1	60^0
1	1	1	0	0	0	0	0	0	0	0

R, Y,B=Red, Yellow, Blue phases,
V_{RN}, V_{YN},V_{BN} = Line to neutral voltages,
V_{RY}, V_{YB}, V_{BR} = Phase to Phase voltages ,M=Magnitude, Ang..=Angle.

This intelligent controller comprise of software, DSP, power circuit and SVPWM in absolute unison. The floating point math algorithm succeeded in optimum designing of FPGA in combination of hardware and software.

The hexagon shown in Figure 4 is clearly describing the changes in every 60° interval of time. The corresponding negative SVPWM are also supplied to the lower IGBT gate terminals.

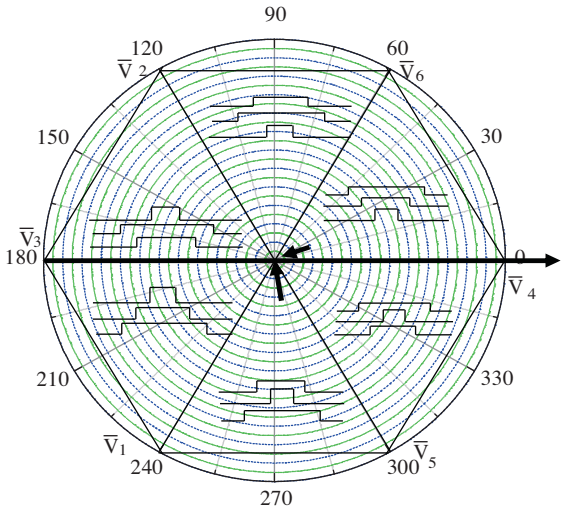

Figure 4. Hexagon of SVPWM, pattern.

3. Cell placement technique

In this section we survey the commercial FPGA's cell placement activation and combination of logic portion of the logic block through which the density and performance of FPGA can be judged. Configurable logic blocks of FPGA are different in terms of size, density and implementation capability. To analyze these differences FPGA can be classified in two categories: fine-grain and coarse-grain. The structural difference can be surveyed as fine-grain having wide CLBs which can be interconnected through program and each switch is controlled by a unique set of configuration memory. While in coarse-grain computing, we have wide data paths available and switches associated with each group are collectively collected by a single set of configuration memory bits. Coarse-grain routing is proved to be more efficient in computing a group of signals from a common source which results in area saving. Fine-grain has proved inefficient utilization of logic blocks. So it is observed that for better performance and for higher efficiency mixed designing should be adopted.

Nowadays, computer aided tools are making it possible to automate the entire layout process that follows the circuit design phase in VLSI design. The input and output logic with pin assignment is done with synthesis and the interconnection is performed through routing channels. But it all depends upon the programming technique followed because the objective of a placement algorithm is to minimize the total chip area and total estimated wire length for net. Configuration, placement and solution are synonym of cell placement technique.

The net list has been shown in Figure 5, the synthesis has been drawn on a Spartan-II xc2s50 FPGA, with the help of VHDL through Xilinx8.1. The architecture mapping for the SVPWM, VHDL program has generated technology schematic and total of 173 activated elements list, is shown in Table 2.

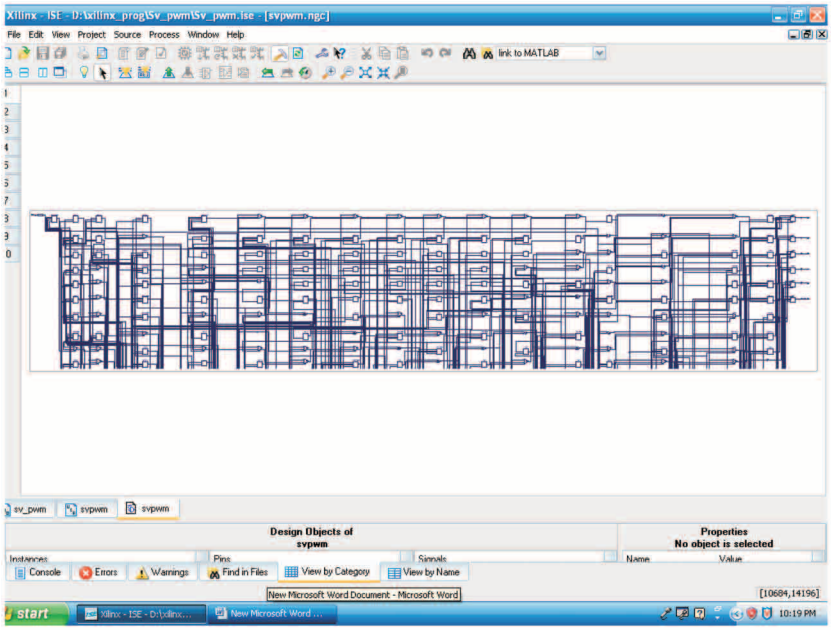

Figure 5. Synthesis Net list.

The block architecture has been analyzed to evaluate the reason for its construction. Some of the blocks from synthesis net list have been discussed to evaluate the reason for providing the desired output. The internal structure of logic block LUT4_L_AABA which is 16 in numbers as evident from Table 2 has been analyzed. It consists of AND gate and INV, two each, and one OR gate connected with output terminal, as shown in Figure 6.

The logic function $f = \overline{a}\overline{b}d + c$ is realized by setting the variables. It carries signals up to the pre-final stage of the program; after which the look up table changes its position by varying the rows in the proceeding columns. This type of LUT is found in the early CLBs of FPGA architecture. The main purpose of this is to produce alternate switching, as can be seen with the truth table given in Table 3.

Another look-up table LUT2_L_E consists of one OR gate, as shown in Figure 7. Its truth table, shown in Table 4, indicates maximum possibility of producing one's. It is clearly evident that LUT2_L_E is contriving the correlation within the program, to transfer input activities to output.

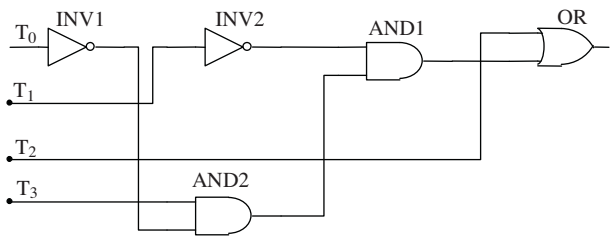

Figure 6. Circuit of LUT4_L_AABA.

Table 2.

Name of Logic block	Specification	Quantity
Look Up Table (LUT)	LUT1_L_2	6
	LUT2_L_E	2
	LUT2_4	3
	LUT2_L_D	3
	LUT2_D_4	5
	LUT2_1	5
	LUT3_FE	2
	LUT3_L_87	3
	LUT3_L_F2	8
	LUT3_L_40	3
	LUT4_L_AABA	16
	LUT4_L_4000	1
	LUT4_L_0001	3
	LUT4_L_0002	5
	LUT4_L_AF23	2
	LUT_E444	1
	LUT4_F544	1
	LUT4_L_7531	1
	LUT4_D_4EFE	1
	LUT4_FFFE	1
	LUT4_L_0213	3
Multiplexer	CY	48
Gates	XOR	10
	AND	3
	INV	9

Table 3. (LUT4_L_AABA).

T_0	T_1	T_2	T_3	D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

The output of look up table (LUT3_L_F2) depends upon T_0 and T_2 which is clearly evident in Figure

8 and Table 5. LUT3_L_F2 has total density 8 out of 173 total no of components. 5 components from those 8 are concentrated in the first column of FPGA architecture.

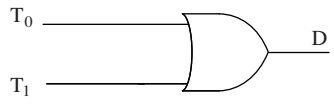

Figure 7. Circuit of LUT2_L_E.

Table 4. IV(LUT2_L_E).

T_0	T_1	D
0	0	0
0	1	1
1	0	1
1	1	1

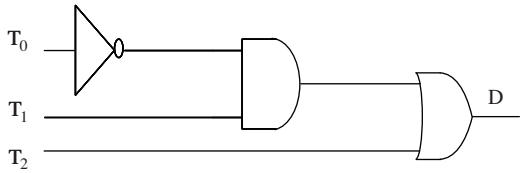

Figure 8. Circuit of LUT3_L_F2.

Table 5. (LUT3_L_F2).

T_0	T_1	T_2	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Multiplexer MUC-CY consists of approximately 28% of the total logic blocks. More number of multiplexer-based logic blocks have an advantage of providing a large degree of functionality with minimum utilization of transistors, but it can be possible with the use of large inputs. These types of blocks are more preferred in FPGA architecture for minimization.

4. Result and discussion

The result can be analyzed in two ways: one is via logic block formation, second is via output wave formation.

The logic blocks discussed in previous sections are connected sequentially through routing. It has been observed that 2-order look up table implementation requires one logic gate, 3-order look up table implementation requires three logic gate and 4-order has four logic gate components. Hence it is results that the number of

memory bits required is directly proportional to the K-factor of LUT and is equal to $G2^k$ bits, where k is the order of LUT and G is the number of logic gate components in the LUT. For example, a 2-order LUT, which has one logic gate, can accommodate 4 bits, similarly a 3-order LUT can have 24 bits and a 4-order LUT can have 64 bits. The result shows that with the increase in the order of k, look up table implementation exhibits high functionality. The number of fractions is also increased. These additional functions are appreciated in logic designs, but are also difficult to apply for a logic synthesis tool. So it is predicted that with the increase in order K i.e 4-LUT & 5-LUT design becomes more complex.

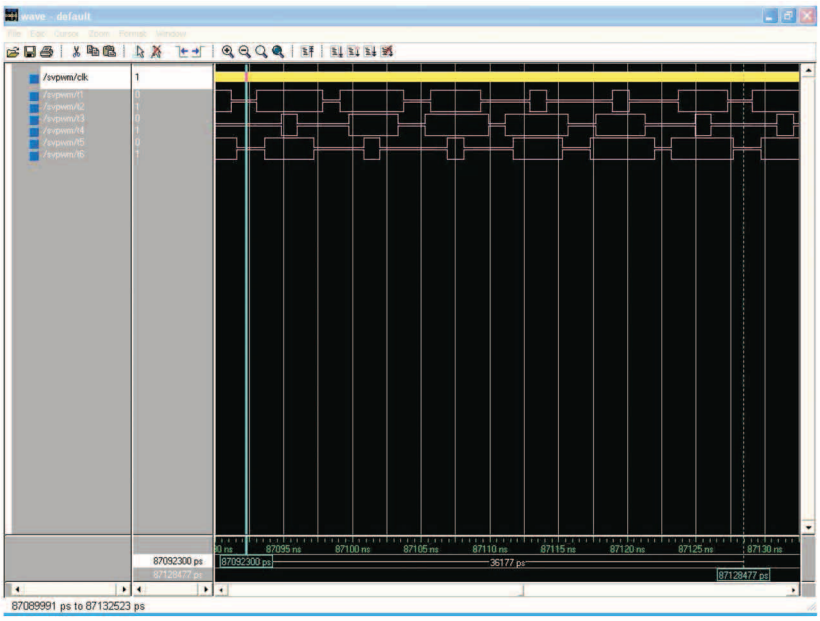

Figure 9. Output wave form of ModelSim5.4a.

Secondly, as shown in Figure 5, for synthesis the program Netlist has a total of 35 (4-LUT)s, 17 (3-LUT)s, 18 (2-LUT)s, 10 XOR, 3 ANDs and 9 INVs. They are so connected that they formed a looping connection between the previous and to the next column. In every block they exchange/replace their position so as to maintain the program active (bit wise) and passing bits to the next connection. The arrangement of components is also creating time delay in the output waves, which is mandatory for the formation of SVPWM wave. XOR gates are absolutely suitable to create the 0-logic for vectors V_0 and V_7 at the beginning and at the end of SVPWM. The output wave form of ModelSim 5.4a shown in Figure 9 proves that the desired result from Figure 4 has been achieved.

5. Conclusion and future work

It is concluded that the synthesis has activated the various components in the internal structure of FPGA. By analyzing the correlation, it is found that the compactness of component placement and desired result oriented architecture is formed. The LUTs have different order and size which further has different gate counts and bit numbers. It is predicted that the placement technique can be modified for the optimum results through genetic algorithm etc.

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