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A novel square-root domain realization of first order all-pass filter

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Abstract

In this paper, a new square-root domain, first order, all-pass filter based on the MOSFET square law is presented. The proposed filter is designed by using nonlinear mapping on the state variables of a state space description of the transfer function. To the best knowledge of the authors, the filter is the first square-root domain first order all-pass structure designed by using state space synthesis method in the literature. The center frequency of the all-pass filter is not only attainable at megahertz frequencies but also tunable by an external bias current. The proposed filter operated 2.5 V supply voltage is constructed by current mirrors, geometric mean circuits, a linear transconductor circuit, and a capacitor. SPICE simulations are given to approve the theoretical analysis.

Key Words: *Square-root domain circuits, All-pass filter, State-space synthesis.*

1. Introduction

There is a growing interest in analog interface circuits that are compatible with CMOS VLSI technology. Compression-expansion, or companding, circuits [1] consisting of log-domain and square-root domain circuits are popular due to suitability for low-voltage, low-power, large dynamic range, high frequency applications and electronic tunability.

The log-domain circuit was first introduced by Adams in 1979 [2]. It was a first order filter having a linear transfer function that could be implemented with nonlinear circuit. In 1990, a class AB translinear integrator that is a special case of log domain integrators [3, 4] was proposed by Seevinck. In the same year the use of the companding in related concept was presented [1]. Then Frey offered the general theory for the design of log domain filters [5]. To design the log domain circuits based on exponential characteristics of the bipolar transistor, state space synthesis method mapped the state variables of a state-space description for

a particular transfer function was stated by Frey in [4, 6]. Furthermore, a log-domain filter implemented in MOSFET operating in subthreshold has been presented in [7]. Since the operating frequency of MOSFET circuits operating in weak inversion is often restricted to kilohertz frequencies, the application of such circuits are limited. Beyond application to CMOS VLSI technology, this technique has been extended to design with saturated MOSFETs used in VLSI systems [8]. When a MOSFET operates in the saturation region, there is a quadratic relationship between the drain current and gate-source voltage. Hence, such circuits are called square-root-domain circuits.

All-pass filters are widely used in many analog signal processing applications. They are also called phase shifters, because they generate frequency-dependent delay while holding the amplitude of the input signal over the desired frequency range [9]. In the literature, there is only one proposed square-root domain all-pass filter: by using N-cell and P-cell exists [10]. In this study, a square-root domain all-pass filter is proposed by mapping to the state variables of a state space description of a linear transfer function, for the first time. The proposed filter has the merit of tunability and integrable by using MOSFET transistors and a capacitor.

2. Circuit design

The present square-root domain first order all-pass filter has been designed by using state space synthesis method. The transfer function of a first order all-pass filter with negative gain is expressed as

$$H(s) = -\frac{s-\omega_0}{s+\omega_0}, \tag{1}$$

where ω_0 is the center frequency of the filter. By using the companion form [11]

$$\dot{x} = -\omega_0 x + 2\omega_0 u \tag{2}$$

$$y = x - u, \tag{3}$$

transfer function (1) can be transformed to

$$C\dot{V}_1 = -\omega_0 C V_1 + 2\omega_0 C u \tag{4}$$

$$y = V_1 - u, \tag{5}$$

where variable x is redefined as the node voltage V_1 across capacitance C, and $C\dot{V}_1$ is the accepted a current flows through capacitor C. Furthermore, assuming that V_1 and u are gate-source voltages of the MOS transistors operating in the saturation region and their drain currents are defined as I_1 and I_u, respectively, equation (4) is reformulated as

$$C\dot{V}_1 = -\omega_0 C\left(\sqrt{\frac{I_1}{\beta}}+V_{TH}\right) + 2\omega_0 C\left(\sqrt{\frac{I_u}{\beta}}+V_{TH}\right), \tag{6}$$

where $I_1 = \beta(V_1 - V_{TH})^2$, $I_u = \beta(u - V_{TH})^2$ and where β and V_{TH} are the device transconductance parameter and the threshold voltage, respectively. Lastly, equation 6 is reconstructed according to currents:

$$I_C = -\sqrt{I_0}\sqrt{I_1} + 2\sqrt{I_0}\sqrt{I_u} + I_{TH} \tag{7}$$

where $I_C = C\dot{V}_1$, $I_0 = \frac{\omega_0^2 C^2}{\beta}$, and $I_{TH} = \omega_0 C V_{TH}$. In this point, the current I_u, can be written as $I_u = 4\beta(u - V_{TH})^2$, so the node equation is modified as

$$I_C = -\sqrt{I_0}\sqrt{I_1} + \sqrt{I_0}\sqrt{I_u} + I_{TH}. \tag{8}$$

With respect to equation (7), we propose an all-pass filter as shown, schematically, in Figure 1. Transistor pairs M_2-M_3, M_4-M_5 and M_6-M_7 are current mirrors to convey square root of the currents. Transistors M_8 and M_9 compose the transconductor circuit to obtain the output signal [12].

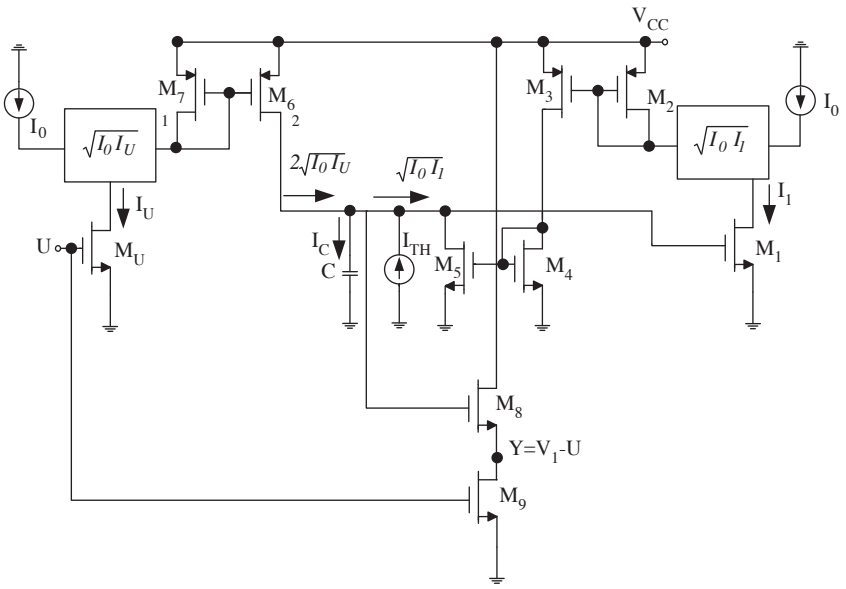

Figure 1. The proposed square-root domain all-pass filter.

3. Simulation results

The circuit was simulated using TSMC 0.25 μm CMOS model parameters in circuit simulator program SPICE with 2.5V supply voltage using a 1.5 pF capacitor. Aspect ratios of the transistors in the filter are given in Table 1. The geometric mean circuit shown in [13] is shown in Figure 2. While the bias current I_0 is 10 μA, the phase response and the gain response of the filter are observed as shown in Figure 3 with ideal response. Theoretically, the center frequency is adjusted to 3.21 MHz; however, the center frequency as determined via the simulation is 3.18 MHz.

Table 1. Aspect ratios of transistors.

M_U, M_1 = 7 μm / 7 μm	M_6 = 0.7 μm / 14 μm
M_1– M_5 = 7 μm / 7μm	M_7–M_9 = 0.7 μm / 7μm

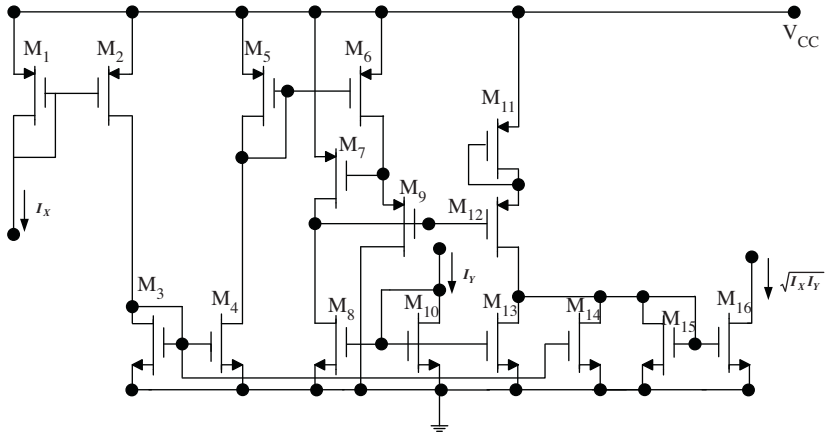

Figure 2. Geometric-Mean circuit as used in [13].

Electronically tunable phase response of the proposed filter for five different bias currents, from 5 μA to 25 μA, is depicted in Figure 4. Figure 5 shows the time domain response of the filter for a bias current of 10 μA and input voltage of 10 mV at 3.21 MHz frequency. This causes 78.07 ns time delay at the filter's output, corresponding to 91.94° phase difference, which is close to the theoretical value of 90°. The total power consumption and the total harmonic distortion were measured as 2.54 mW and 1.41%, respectively. The dependence of the output harmonic distortion of presented filter on input signal amplitude is illustrated in Figure 6. As shown in this figure, THD increases with input signal. As such, input signal must be 200 mV or less to avoid output distortion.

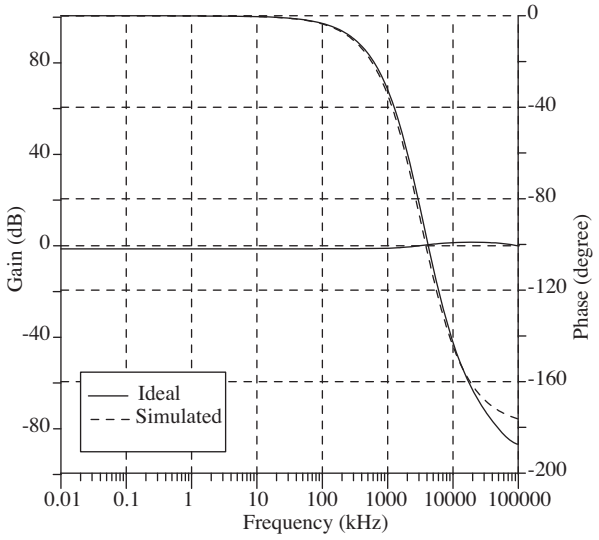

Figure 3. Gain and Phase response of the first-order all-pass filter.

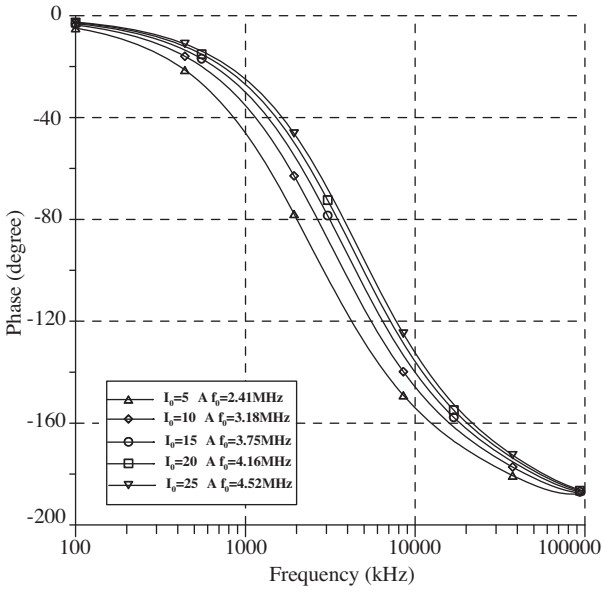

Figure 4. Electronically tunable phase response of the first-order all-pass filter.

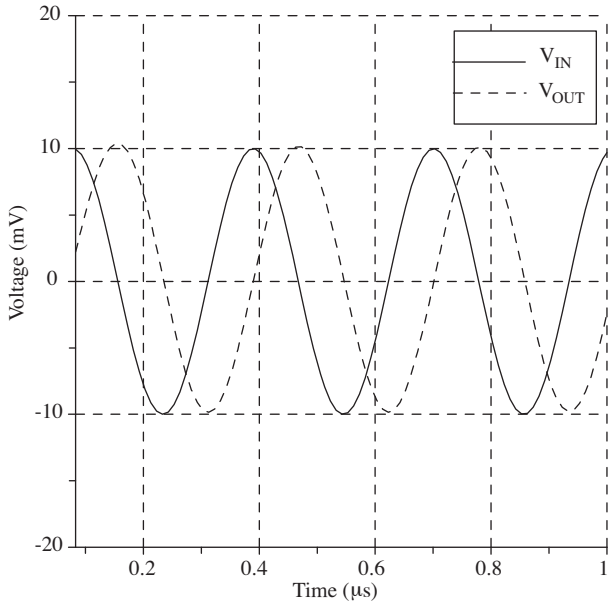

Figure 5. Time domain response of the proposed all-pass filter.

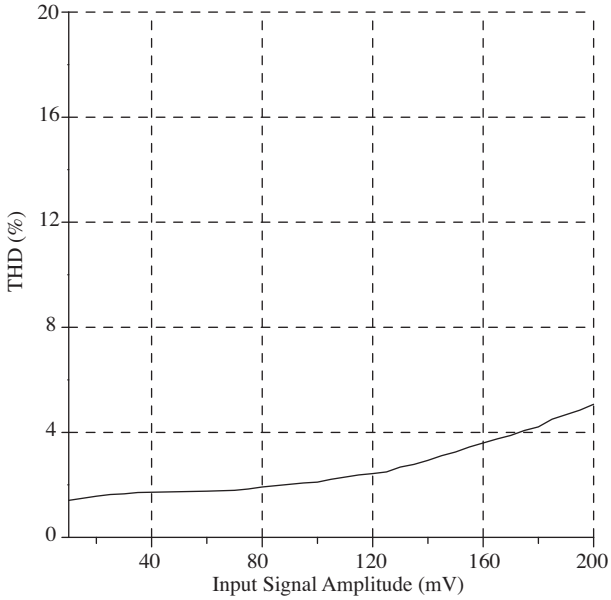

Figure 6. Total harmonic distortion (THD) as a function of input signal amplitude at 3.21 MHz.

4. Conclusion

In this work, a novel square-root domain first-order all-pass filter has been proposed. It is systematically derived using state-space synthesis technique, and is the first such all-pass filter in the literature. The filter circuit has simple structure and is suitable for integrated circuit implementation since it only consists of a capacitor and MOS transistors. The most important feature of the circuit is electronic tunability, that is, the phase response of the circuit can be controlled by an external current at megahertz frequencies. Thus, the proposed first-order all-pass filter can be used as an electronically controllable phase shifter. It also inherited advantage of companding circuit such as large dynamic range, low total harmonic distortion. Theoretical analysis and design are confirmed by SPICE simulations.

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