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Small signal analysis for DC bus voltage disturbance resistance of voltage source converter

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Abstract: The DC bus voltage of the voltage source converter (VSC) is prone to large fluctuation and even to losing its stability for the large mutation of grid voltage or DC-link loads. First the characteristics of two-step transmission to power in the VSC are analyzed, proving that it is inevitable for DC bus voltage fluctuation to occur when grid voltage or DC-link loads mutate. A new two-step feedforward control strategy is then put forward for curbing the fluctuation, which overcomes the shortcoming by which the traditional feedforward control strategy is affected for the performance of current control. The small signal models of nonfeedforward control, traditional feedforward control, and two-step feedforward control are established respectively for comparing their performance. It is certified that the two-step feedforward control maximizes the stability of the bus voltage without affecting current control. Finally, the experimental results verify the correctness of the new strategy and the theoretical analysis.

Key words: DC bus voltage, small signal model, power balance, feedforward control, disturbance resistance

1. Introduction

The three-phase voltage source converter (VSC) [1–3] has widespread applications, including active power filters, unified power flow control, high voltage direct current transmission, and power transmission for solar, wind, and other renewable energies. It can be also foreseen that the VSC could become the main connection device of future smart grid technologies, such as in grid energy storage, flexible power transmission, renewable energy generation, controllable loads, etc. [4].

The ideal condition of the grid is generally presumed to design the VSC control. However, in the actual grid, grid voltage usually fluctuates because of grid faults and switching large loads. At the same time, there is a large mutation of the DC-link supplies or loads in the converter DC side of VSC. When these problems occur, the DC bus voltage of the VSC will fluctuate more or less, and may even be out of control [5], for which better disturbance resistance for the VSC is required.

The traditional dual-loop control [6,7] needs to pass control instructions through the voltage regulator and current regulator in order to control the DC bus voltage, which leads greatly to cascaded delay and the overshoot. Thus, feedforward control [8,9] was proposed to improve the response over certain regulators. At present, feedforward control includes two major control modes. In one mode, a feedforward branch is added to the output of the voltage regulator, based on the power balance on both sides of VSC. This mode is advantageous to the current limiting. However, the response is partially affected so as to weaken disturbance resistance because the instructions need to pass the current regulator. A variable structure control is added to further improve the

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response in the literature [10]. The other mode is straight control of the DC-link capacitor current of the VSC [11,12]. This mode easily amplifies the disturbance for introducing the differential into the feedforward branch. Moreover, this mode easily causes some errors because the DC-link capacitor current is not directly detected, only estimated.

In addition to improving control strategies, scholars from different countries have been studying the disturbance resistance from the angle of system parameter design, generally with small signal analysis [13–17]. In the literature [14], the small signal model of VSC is established to design the parameters of regulators in traditional dual-loop control for its stability and performance. In the literature [16,17], a small signal model is implemented for the photovoltaic grid-connected inverter with LCL filter. Considering the factors such as disturbance resistance of DC bus voltage, characteristics of photovoltaic array, inductive reactance, and so on, the control sensitivity of the inverter is analyzed.

From the perspective of the power balance on both sides of the VSC, this paper first comprehensively analyzes the nature of the DC bus voltage fluctuation and its suppression principle. A new feedforward control to curb DC bus voltage fluctuation is put forward, which is called two-step feedforward control in this paper. Small signal models of nonfeedforward control, traditional feedforward control, and two-step feedforward control are established. The performances of the three control strategies are carefully compared by small signal analysis in the time and frequency domains. Finally, the proposed control strategy and theoretical analyses are verified through experimental results.

2. Suppression principle of DC bus voltage fluctuation

The three-phase VSC is shown in Figure 1. The converter grid side is connected to the grid through the LCL filter including converter side inductance L_T, grid-side inductance L_g, filter capacitor C_f, and damping resistance R. The converter DC side is connected to the DC-link supplies or loads through the DC-link capacitor C.If the grid and the DC-link supplies or loads are stable, sine grid current and smooth DC bus voltage could be produced by controlling six IGBTs (S_{a1}, S_{a2} S_{b1}, S_{b2}, S_{c1}, S_{c2}).

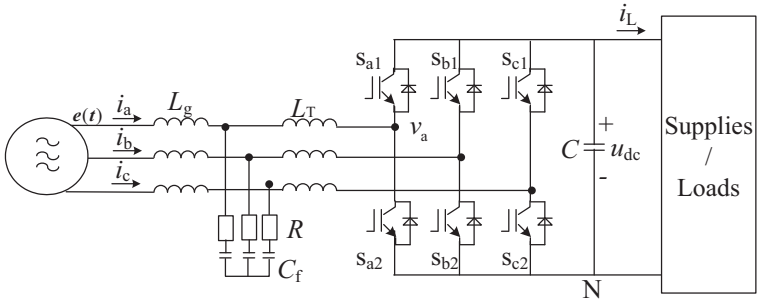

Figure 1. Three-phase voltage source converter.

However, the VSC is often in complex surroundings, as shown in Figure 2. Grid voltage in the connection between the VSC and the grid could fluctuate from time to time, for example when some generators and large loads in the grid are switched. With a large number of intermittent new energies and nonlinear large loads, sudden changes of grid voltage happen more and more. The DC-link supplies or loads could also change randomly. The VSC, and specifically its DC bus voltage, is seriously affected by these problems.

The equivalent topological structure of the VSC is shown in Figure 3. The converter part is respectively treated as the controlled voltage sources and controlled current sources on the grid side and DC side [18]. The

widely used LCL filter is replaced by a pure inductance filter in Figure 3 because the effect of the capacitor in LCL filters can be ignored at low frequency [19]. Assuming that all switches and sources are ideal and balanced, the equation sets of the VSC are given based on Kirchhoff's law.

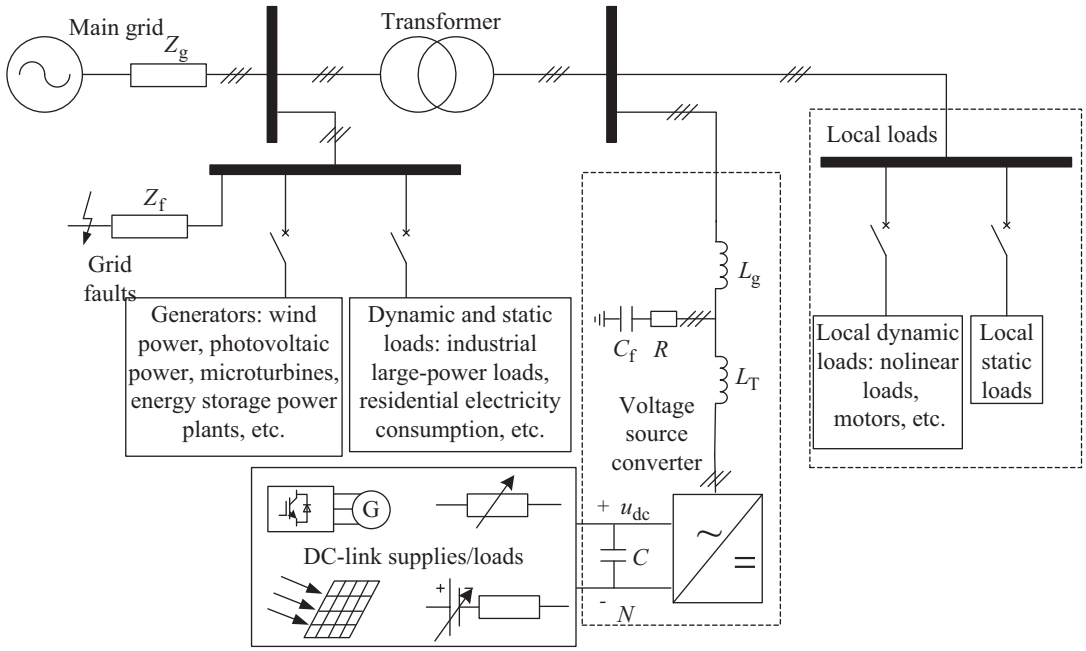

Figure 2. Grid and DC-link surrounding of VSC.

$$e_k = L\frac{di_k}{dt} + u_{dc}d_k - \frac{u_{dc}}{3}\sum_{k=a,b,c} d_k \tag{1}$$

$$C\frac{du_{dc}}{dt} = \sum_{k=a,b,c} i_k d_k - i_L \tag{2}$$

Where:

e_k, i_k is k phase grid voltage and k phase grid current, respectively ($k = a, b, c$);

L is the inductance of filter ($L{=}L_g + L_T$ if LCL filter is used);

u_{dc} is the DC bus voltage;

C is the DC-link capacitor;

d_k is the duty ratio of k phase; and

i_L is the DC-link current.

The zero sequence voltage produced in some modulation algorithms is not involved in energy transmission, so the zero sequence voltage $\frac{u_{dc}}{3}\sum_{k=a,b,c} d_k$ needs be abstracted from the converter grid-side voltage $u_{dc}d_k$ in Eq. (1). It can be seen from Figure 3 that the transmitted energy between the grid side and load side must pass the converter grid side and converter DC side, for which the VSC has the characteristic of two-step energy transmission. The time constant of the inductance is smaller than that of the DC-link capacitor, and leading to that the following speed of the grid current is faster than that of the DC bus voltage. Therefore, after grid-side power p_1 or load-side power p_4 mutates, the duty ratio would be first changed to get the grid current required

according to Eq. (1) and to realize the balance between p_1 and p_4. However, at this time the duty ratio cannot meet the demand that converter grid-side power p_2 or converter DC-side power p_3 synchronously follow with p_1, and even oppositely, resulting in the inconsistency of power on both ends of the DC-link capacitor and in the DC bus voltage fluctuation. The details will be explained in the following text. The equations of power at all steps are shown in Eqs. (3)–(5).

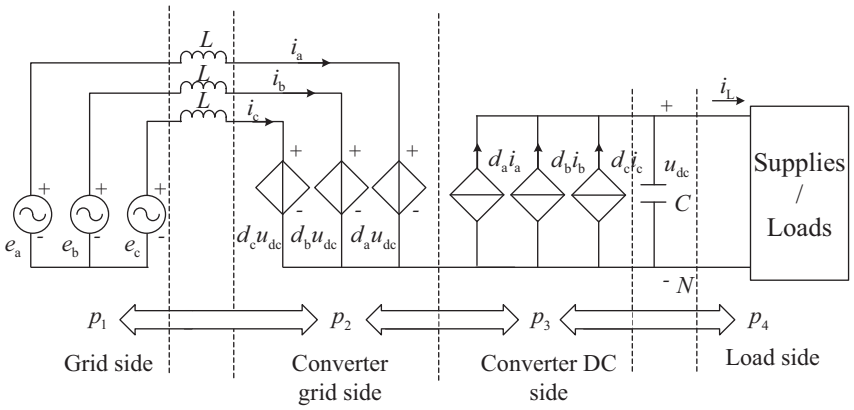

Figure 3. Equivalent topological structure of three-phase VSC.

$$p_1 = e_a i_a + e_b i_b + e_c i_c \tag{3}$$

$$p_2 = p_3 = u_{dc}(d_a i_a + d_b i_b + d_c i_c) \tag{4}$$

$$p_4 = u_{dc} i_L \tag{5}$$

Through the coordinate transformation, the mathematical model is transformed from the three-phase static coordinate system to the synchronous rotating coordinate system. If the $d$axis of the rotating coordinate system is set on the vector of grid voltage and the converter works under the unit power factor, the mathematical model can be simplified into:

$$L\frac{di_d}{dt} = e_d - u_d \tag{6}$$

$$L\frac{di_q}{dt} = -u_q - \omega L i_d \tag{7}$$

$$C\frac{du_{dc}}{dt} = \frac{3}{2}.\frac{u_d}{u_{dc}} i_d - i_L \tag{8}$$

$$u_d = u_{dc} d_d \tag{9}$$

$$u_q = u_{dc} d_q \tag{10}$$

$$p_1 = \frac{3}{2} e_d i_d \tag{11}$$

$$p_2 = p_3 = \frac{3}{2} u_d i_d \tag{12}$$

Where:

e_d, i_d is grid voltage and grid current in d axis, respectively;

e_q, i_q is grid voltage and grid current in q axis, respectively;

d_d, d_q is the duty ratio in d axis and in $q$axis, respectively; and

u_d, u_q is converter grid-side voltage in d axis and in q axis, respectively.

According to Eqs. (6)–(8), the simplified converter circuit diagram in the rotating coordinate system is drawn as shown in Figure 4. It can be seen that i_d and u_{dc} can only be controlled by u_d. If load-side power increases, u_d needs to be reduced so as to get the bigger i_d as soon as possible from Eq. (6). The required current i_d is shown in Eq. (13). Until the time that u_d is changed to be equal to e_d for stabilizing i_d, the converter DC-side power is equal to the load-side power. The DC bus voltage would drop because converter DC-side power by Eq. (12) is less than the load-side power in this process. This process can be more clearly shown if using the vectors as shown in Figure 5.

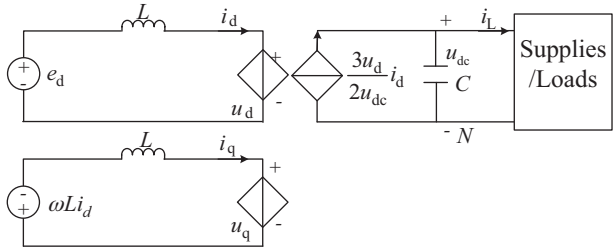

Figure 4. Simplified converter circuit diagram in the rotating coordinate system.

$$G_3 = i_d = \frac{u_{dc} i_L}{3e_d/2} \tag{13}$$

Figure 5 shows the changing process of VSC space vectors in the rectification mode and in unit power factor, so as to adapt respectively to the mutation of the grid voltage or DC-link loads. If the $d$axis of the rotating coordinate system is set on the vector of grid voltage, E, I, and U respectively indicate grid voltage vector, grid current vector, and converter grid-side voltage vector before change; E',I', and U_2' respectively indicate grid voltage vector, current vector, and converter-grid-side voltage vector after change; u_d and U_1' respectively indicate the converter grid-side voltage subvector in the d axis and the converter grid-side voltage vector, which are used to obtain the required grid current; and $u_d^{'}$ and $U'_{\max}$ respectively indicate the maximum converter grid-side voltage subvector in the d axis and the maximum converter grid-side voltage vector, which are provided to obtain the maximum changing of grid current. The shaded part belongs to the optional range of U_1'.

In Figures 5a and 5b, when grid voltage drops or load-side power increases, grid-side power will be less than the load-side power. In order to increase grid-side power, namely to the bigger amplitude of I, the amplitude of u_d needs to be less than the amplitude of E, even in the opposite direction. At this time, because the grid current is not changed in time, the vector of inductance voltage $j\omega LI$ is unchanged, and U_1' is synthesized by u_d and $j\omega LI$. The DC bus voltage would drop because converter DC-side power by Eq. (12) is obviously less than the load-side power in the two processes. Meanwhile, U_1' can be modulated at the utmost to the edge of the hexagon space voltage vector graph, such as $U'_{\max}$, so the higher the DC bus voltage is, the lower the modulation ratio is, while the wider U_1' has the range of choice and the DC bus voltage can be more easily controlled.

In Figures 5c and 5d, in order to decrease the amplitude of I, the amplitude of u_d should be more than the amplitude of E. Similarly, U_1' can be modulated at the utmost to the edge of the hexagon space voltage vector graph. The DC bus voltage would rise because converter DC-side power by Eq. (12) is obviously more

than the load-side power in the two processes. Compared with Figures 5a and 5b, U_1' has the narrower range of choice and the DC bus voltage is not easier to control.

However, in the inversion mode, due to the change of the current direction, it is opposite to the analytical conclusions of rectification mode, and this paper herein does not mention it in detail. The converter DC-side power is already unequal to the load-side power in these processes, so the DC bus voltage fluctuation is inevitable. It is necessary to cut down the time of these processes as soon as possible.

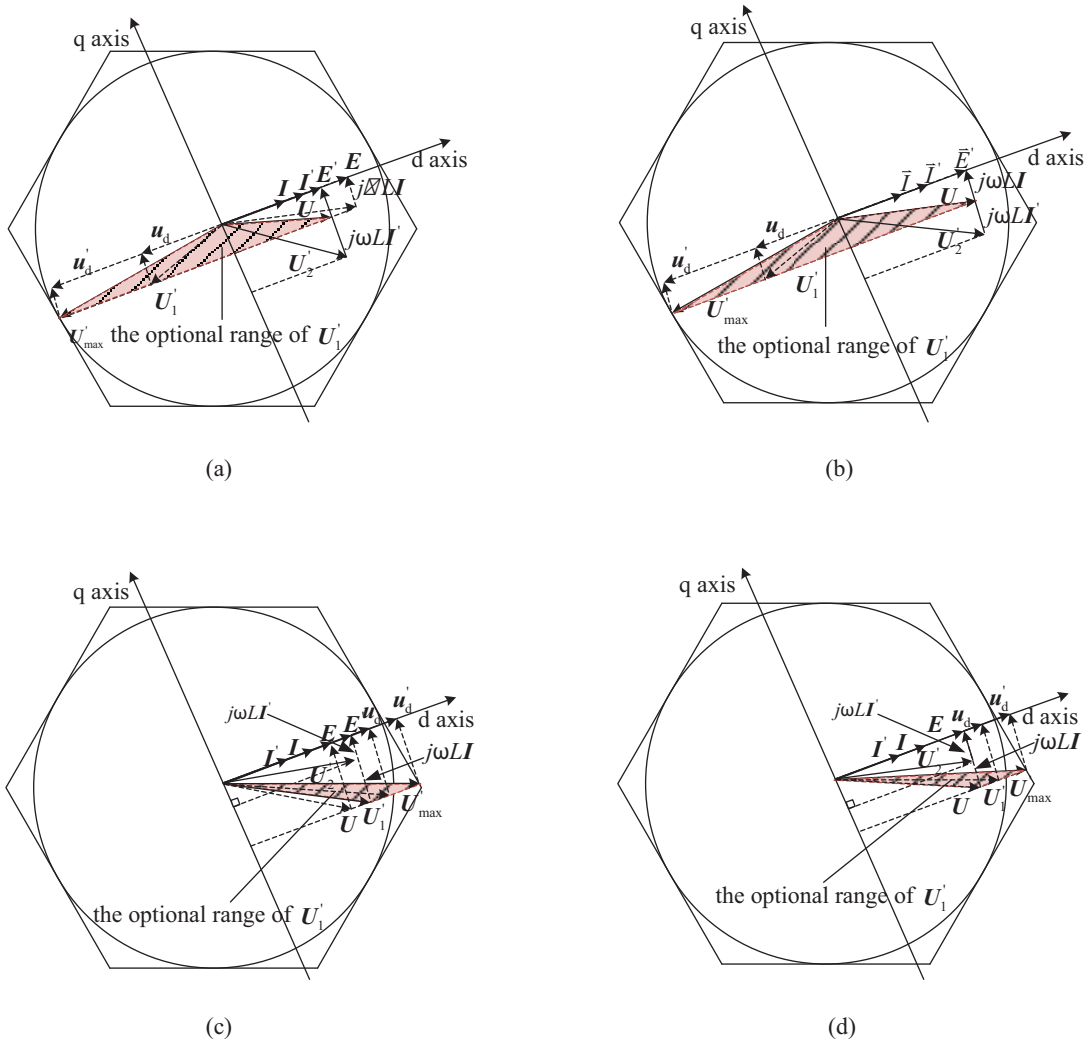

Figure 5. Variation diagram of VSC space vectors in the rectification mode:(a) grid voltage drops;(b) load-side power increases;(c) grid voltage rises;(d) load-side power decreases.

3. A two-step feedforward strategy for suppressing DC bus voltage fluctuation

Amplitude and time of the fluctuation depend on not only the time constant of the inductance and DC-link capacitor, but also the response speed of the control system. On the basis of the steady-state balance principle of grid-side power p_1 and load-side power p_4, the traditional strategy [8] directly feeds forward the change signal of the converter loads and grid voltage to the given current. The feedforward calculation is shown in Eq. (13), and the control block diagram is shown as the first-step feedforward branch in Figure 6. This strategy reduces

the response time of the outer voltage loop. Assuming that the grid current can be changed instantaneously, the DC bus voltage would not fluctuate [14]. However, because the given current must pass the current regulator to produce a voltage vector, and other performances of the current loop should be considered in the design of this regulator, some rapidity is lost to affect the disturbance resistance of the DC bus voltage.

Eq. (6) is converted to linearize the current change in a switching cycle T_s, as shown in Eq. (14). If the converter grid-side voltage subvector u_d in the d axis is adaptive to the mutation of DC-link loads or grid voltage, the current change could be completed in a switching cycle, which is calculated by Eq. (15).

$$u_d = e_d - L\frac{\Delta i_d}{T_s} \tag{14}$$

$$\Delta i_d = \frac{u_{dc} i_L}{3e_d/2} - i_d \tag{15}$$

Eq. (15) represents the difference between the required current and the actual current after the mutation of the grid voltage or DC-link loads, which is zero when the converter is stable. Eqs. (14) and (15) are fed forward to the given voltage in the d axis, as shown in the dotted portion of Figure 6, forming the second-step feedforward branch. The current regulator has a certain proportionality coefficient, equivalent to a part of the feedforward component, so the feedforward coefficient $k = L/T_s$ is the proportionality coefficient of the current regulator, so as to give full play to the maximum control performance of disturbance resistance of the converter and to achieve the ideal effect of disturbance resistance of the DC bus voltage.

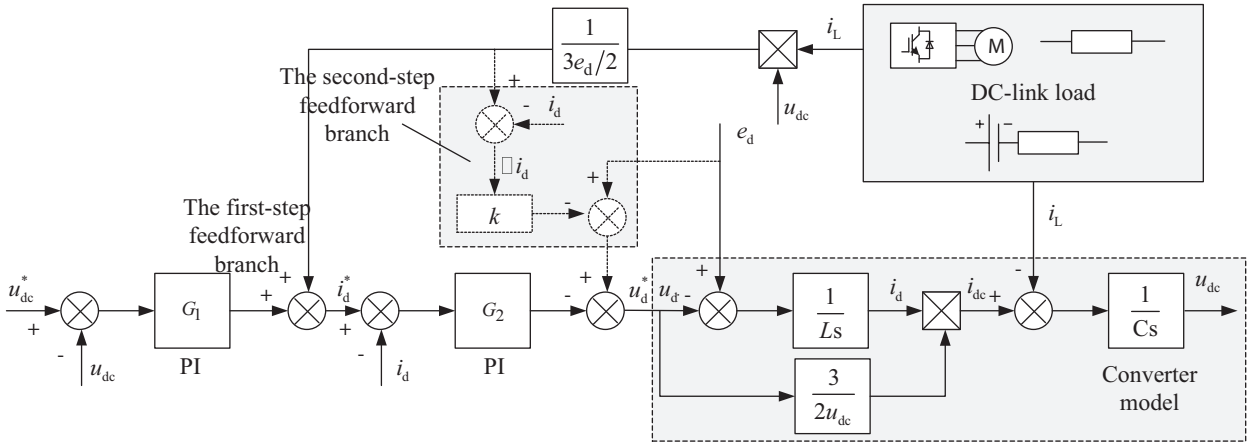

Figure 6. Two-step feedforward control block diagram

4. Analysis based on the small signal model

4.1. Small signal modeling

In order to analyze the performance of the new two-step feedforward control strategy, the small signal model is established for the VSC. In all cases any variable is represented as $x = \bar{X} + \hat{x}$, $\bar{X}$ being the steady-state value around an operation point and $\hat{x}$ the small signal term. Nearby the static working point, the small signal

disturbance is made, given as follows.

$$\begin{cases} i_d = \bar{I}_d + \hat{i}_d \\ e_d = \bar{E}_d + \hat{e}_d \\ u_d = \bar{U}_d + \hat{u}_d \\ u_{dc} = \bar{U}_{dc} + \hat{u}_{dc} \\ i_L = \bar{i}_L + \hat{i}_L \end{cases} \tag{16}$$

It is respectively substituted into Eqs. (6) and (8). After sorting, the small signal model in the d axis is achieved.

$$\begin{cases} L\frac{d\hat{i}_d}{dt} = \hat{e}_d - \hat{u}_d \\ (Cs+\frac{3}{2}ab)\hat{u}_{dc} = \frac{3}{2}b\hat{u}_d + \frac{3}{2}a\hat{i}_d - \hat{i}_L \end{cases} \tag{17}$$

From Eq. (17):

$$a = \bar{E}_d/\bar{U}_{dc} \tag{18}$$

$$b = \bar{I}_d/\bar{U}_{dc} \tag{19}$$

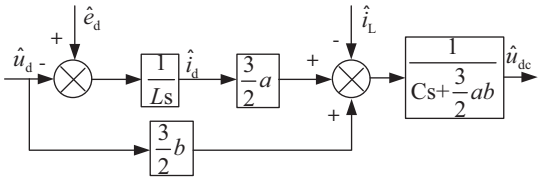

Figure 7. Converter block diagram based on small signal model.

According to Eq. (17), the converter block diagram based on the small signal model can be obtained, as shown in Figure 7. Similarly, the small signal model of the control part conducted in Figure 6 is respectively given.

$$\begin{cases} i_d^* = \bar{I}_d^* + \hat{i}_d^* \\ u_d^* = \bar{U}_d^* + \hat{u}_d^* \\ u_{dc}^* = \bar{U}_{dc}^* + \hat{u}_{dc}^* \end{cases} \tag{20}$$

Because u_{dc}^* can be seen as a given constant in the system at the time of the mutation, $\hat{u}_{dc}^*$ can be given as zero. The small signal formula is respectively conducted for the first-step and second-step feedforward branches, i.e. $\hat{G}_3$ and $\hat{G}_4$, respectively, as shown in Eq. (21).

$$\begin{cases} \hat{G}_3 = \frac{2}{3a}\hat{i}_L + b\hat{u}_{dc} - \frac{b}{a}\hat{e}_d \\ \hat{G}_4 = \hat{e}_d - k(\frac{2}{3a}\hat{i}_L + b\hat{u}_{dc} - \frac{b}{a}\hat{e}_d - \hat{i}_d) \end{cases} \tag{21}$$

From $\hat{G}_4$, it can be seen that $\hat{i}_d$ is feedback to $\hat{u}_d^*$, so the current loop has two-fold feedback characteristics. Figure 8 shows the block diagram for current loop control based on the small signal model. Disregarding the effect of disturbance quantity and PWM delay, the open-loop transfer function of the current loop is shown in Eq. (22). In traditional control, the open-loop transfer function is as shown in Eq. (23).

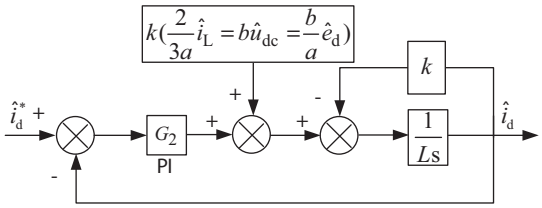

Figure 8. Block diagram for current loop control based on small signal model.

$$\frac{\hat{i}_d}{\hat{i}_d^*} = \frac{G_2}{Ls+k} \tag{22}$$

$$\frac{\hat{i}_d}{\hat{i}_d^*} = \frac{G_2}{Ls} \tag{23}$$

Again, according to Eqs. (20) and (21), the small signal formulas of the given current and the given voltage in the d axis can be respectively achieved, as shown in Eq. (24).

$$\begin{cases} \hat{i}_d^* = G_1(0-\hat{u}_{dc}) + \hat{G}_3 \\ \hat{u}_d^* = -G_2(\hat{i}_d^* - \hat{i}_d) + \hat{G}_4 \end{cases} \tag{24}$$

By the new simultaneous equations (Eqs. (17), (21) and (24)), the small signal model of DC bus voltage is achieved, as shown in Eq. (25). In the same method, the small signal models of DC bus voltage are achieved under nonfeedforward control and traditional feedforward control (the first-step feedforward branch), respectively shown in Eqs. (26) and (27).

$$\hat{u}_{dc} = \frac{\frac{3}{2}bLs(1+\frac{bk}{a}+\frac{b}{a}G_2)\hat{e}_d - Ls(1+\frac{bk}{a}+\frac{b}{a}G_2)\hat{i}_L}{(G_2+Ls+k)(Cs+\frac{3}{2}ab)+\frac{3}{2}(a-bLs)(G_1G_2-bk-bG_2)} \tag{25}$$

$$\hat{u}_{dc} = \frac{\frac{3}{2}b(Ls+G_2)\hat{e}_d - (Ls+G_2)\hat{i}_L}{(G_2+Ls)(Cs+\frac{3}{2}ab)+\frac{3}{2}(a-bLs)G_1G_2} \tag{26}$$

$$\hat{u}_{dc} = \frac{\frac{3}{2}bLs(1+\frac{b}{a}G_2)\hat{e}_d - Ls(1+\frac{b}{a}G_2)\hat{i}_L}{(G_2+Ls)(Cs+\frac{3}{2}ab)+\frac{3}{2}(a-bLs)(G_1G_2-bG_2)} \tag{27}$$

Through Eqs. (25)–(27), it can be seen that in the three control strategies, grid voltage and DC-link loads have the same law of disturbance for DC bus voltage, and the difference between their gains is only b times. As is known, when the grid current is small, the disturbance influence of grid voltage on the DC bus voltage is far less than that of DC-link loads.

4.2. System performance analysis based on small signal model

Because the grid voltage mutation has the same law of disturbance for DC bus voltage as the DC-link mutation, the following section will take an instance of DC-link mutation to analyze the performances of the three strategies, and parameters of the VSC are shown in Table 1. If the LCL filter with total filtering inductance of 3 mH and switching frequency of 5 kHz is used, $L/T_s = 15$.

Eqs. (25)–(27) are applied to achieve the Bode diagram for the small signal models of DC bus voltage under three strategies (load part), as shown in Figure 9. It can be seen that under the nonfeedforward control,

the low-frequency gain is obviously more than that under the feedforward control. Under the traditional feedforward control, the low-frequency gain decreases with the increase of proportional coefficient kp_2 of the current regulator. The Bode diagram of two-step feedforward control ($kp_2 = 5$) basically coincides with the Bode diagram of the traditional feedforward control ($kp_2 = 15$), both of which indicate the minimal disturbance for DC bus voltage. Nonetheless, at this point, the kp_2 of two-step feedforward control is far less than that of traditional feedforward control.

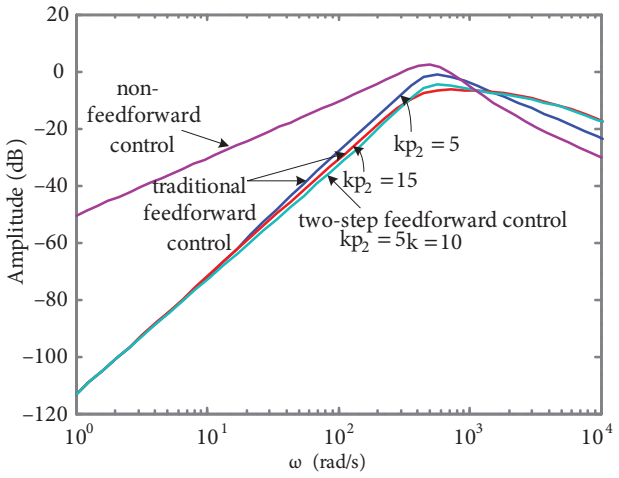

Figure 9. Bode diagram for small signal models of DC bus voltage fluctuation under three strategies (load part).

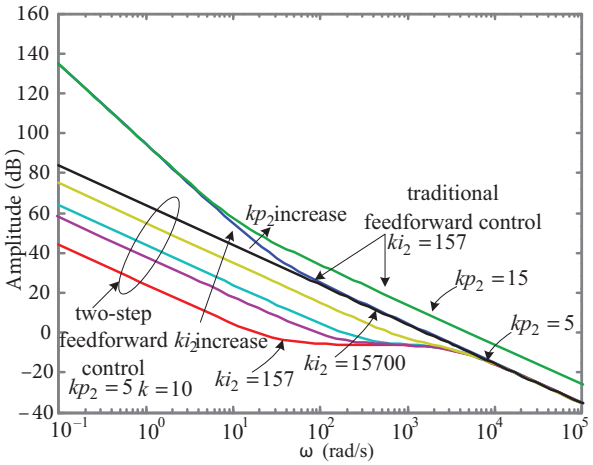

Figure 10. Open-loop Bode diagram for current loops under two feedforward control strategies based on small signal model.

Eqs. (22) and (23) are applied to obtain the open-loop Bode diagram for current loops under two feedforward control strategies based on the small signal model, as shown in Figure 10. Under the traditional feedforward control, the cutoff frequency point increases with the increase of kp_2, and grid current is more easily interfered with by the high frequency. In addition, according to the analysis in Figure 9, the two-step feedforward control does not increase kp_2 to reduce the low-frequency gain of the small signal model of DC bus voltage, so the high-frequency gain of the current loop is consistent with the traditional feedforward control ($kp_2 = 5$). However, the feedforward coefficient k in Figure 10 generates the damping effect to drop the low-frequency gain of current loop, but this gain can be compensated by increasing the integral coefficient ki_2 of the current regulator. The open-loop Bode diagram for the current loop under the two-step feedforward control ($kp_2 = 5$ and $ki_2 = 15700$) is basically consistent with that under the traditional feedforward ($kp_2 = 5$ and $ki_2 = 157$) so as to realize the study purposes, i.e. the current loop performance is unchanged and disturbance resistance of DC bus voltage is improved.

Figure 11 shows the root locus of the small signal model of DC bus voltage under the two-step feedforward control (kp_1 from 0.25 to 20). At this moment, $ki_1 = 825$, $kp_2 = 5$, and $ki_2 = 15700$, and when kp_1 is between 1.25 and 10.75, the system is stable and has large bandwidth. Figure 12 shows the response of DC bus voltage at the DC-link load step. Under nonfeedforward control and traditional feedforward control, the parameter $ki_2 = 157$; under two-step feedforward control, the parameter $ki_2 = 15700$; and other parameters are consistent. It can be found that under two-step feedforward control, the amplitude and the stability time of DC bus voltage fluctuation are obviously less than those of the other two control strategies.

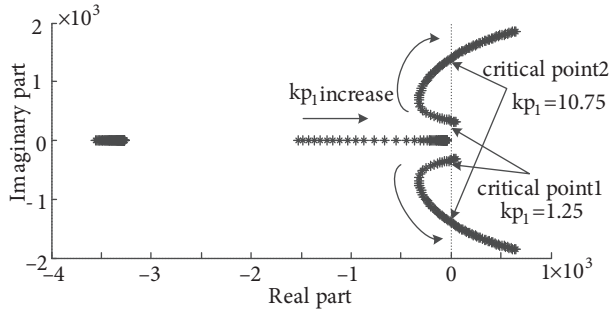

Figure 11. Root locus of the small signal model of DC bus voltage under the two-step feedforward control (kp_1 from 0.25 to 20) (load part).

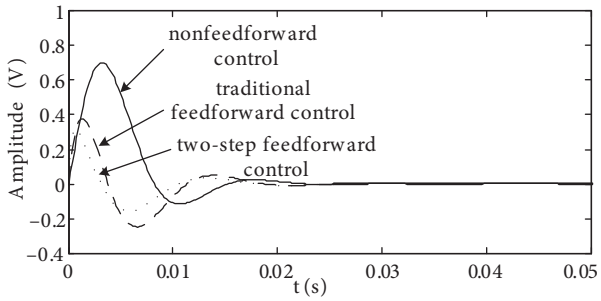

Figure 12. Response of DC bus voltage (unit step of load section).

5. Experimental results

An experimental platform of a 2.5 kW VSC is set up, and the parameters are shown in Table 1. The principle diagram of the experimental platform is shown in Figure 13. To reduce the inductance value and improve the speed of current response, this experiment adopts the LCL filter. The voltage regulator parameters of three control strategies, i.e. nonfeedforward control, traditional feedforward control, and new two-step feedforward control, are $kp_1 = 3.3$ and $ki_1 = 825$. Because grid voltage mutation and load mutation have the same disturbance law for DC bus voltage, this experiment will take DC-link load mutation as an example to respectively validate the system response when using these three control strategies. DC-link loads R_{L1} continue working until the end of the experiment, and DC-link loads R_{L2} act as the mutated loads.

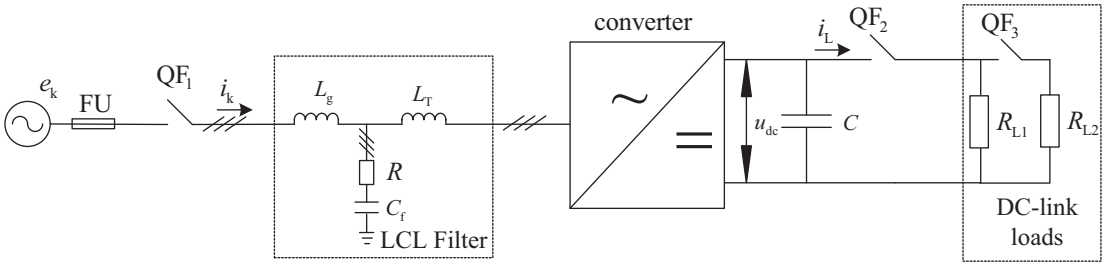

Figure 13. Principle diagram of the experimental platform.

Figure 14 shows a photo of the experiment platform. The main controller chip is TI DSP TMS320F2812. IGBTs not seen under their driver circuitries use the BSM50GB120DLC IGBT from Infineon Technologies AG. Driver circuitry is formed by a Dual Scale Driver 2SD315A from CONCEPT and its extension board. DC-link loads in the other electric cabinet are not shown in the photo.

Figure 15 shows the diagram for response waveforms of the three control strategies when DC-link loads mutate (approximately 0.1–2 kW). To test and verify the control characteristics of the DC bus voltage of the three control strategies in the same situation, the characteristics of current loop must be basically consistent. Based on the analysis of current loop characteristics in Figure 10, in Figures 15a, 15b and 15c, the proportional coefficient of the current regulator is taken as $kp_2 = 5$; in the first two figures, the integral coefficient of the current regulator is taken as $ki_2 = 157$; in Figure 15c, the integral coefficient of the current regulator is taken as $ki_2 = 15700$. It can be seen that, under two-step feedforward control, the amplitude of DC bus voltage dip

is minimum, but that of DC bus voltage dip under nonfeedforward control is maximum. When the proportional coefficient of the current regulator of the traditional feedforward control is taken as $kp_2 = 15$, as shown in Figure 15d, the amplitude of DC bus voltage dip is almost consistent with that under two-step feedforward control.

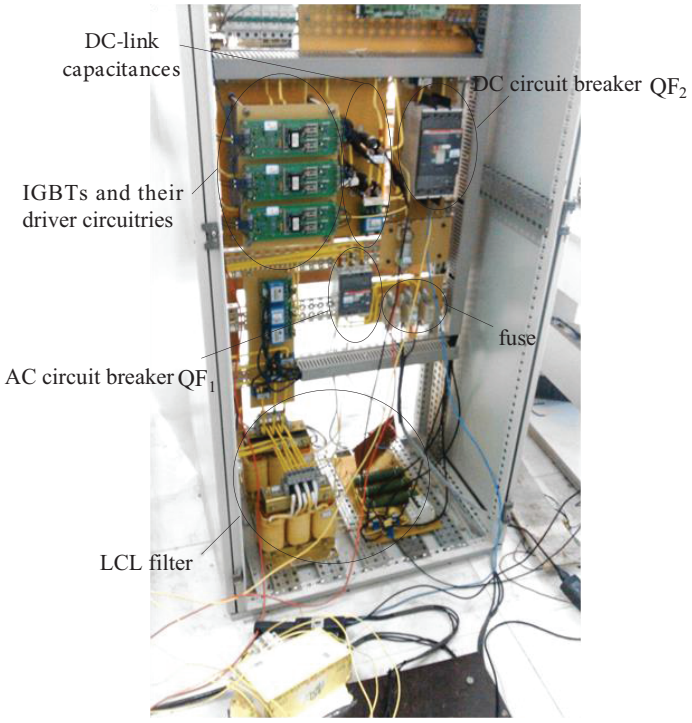

Figure 14. The photo of the experimental platform.

Table 1. System parameters of the experimental platform of 2.5 kW VSC.

Parameters	Numerical value
LCL filter converter-side inductance L_T (mH)	2
LCL filter grid-side inductance L_g (mH)	1
LCL filter capacitor C_f (μF)	4.75 (Δ type)
LCL filter damping resistance R (Ω)	5
DC-link capacitor C (μF)	3.3
DC bus voltage u_{dc} (V)	300
DC-link loads R_{L1} (Ω)	1000
DC-link loads R_{L2} (Ω)	50
Peak of k phase grid voltage e_k (V)	81
Rated peak t of k phase grid current i_k (A)	20
Switching frequency f_{sw} (kHz)	5

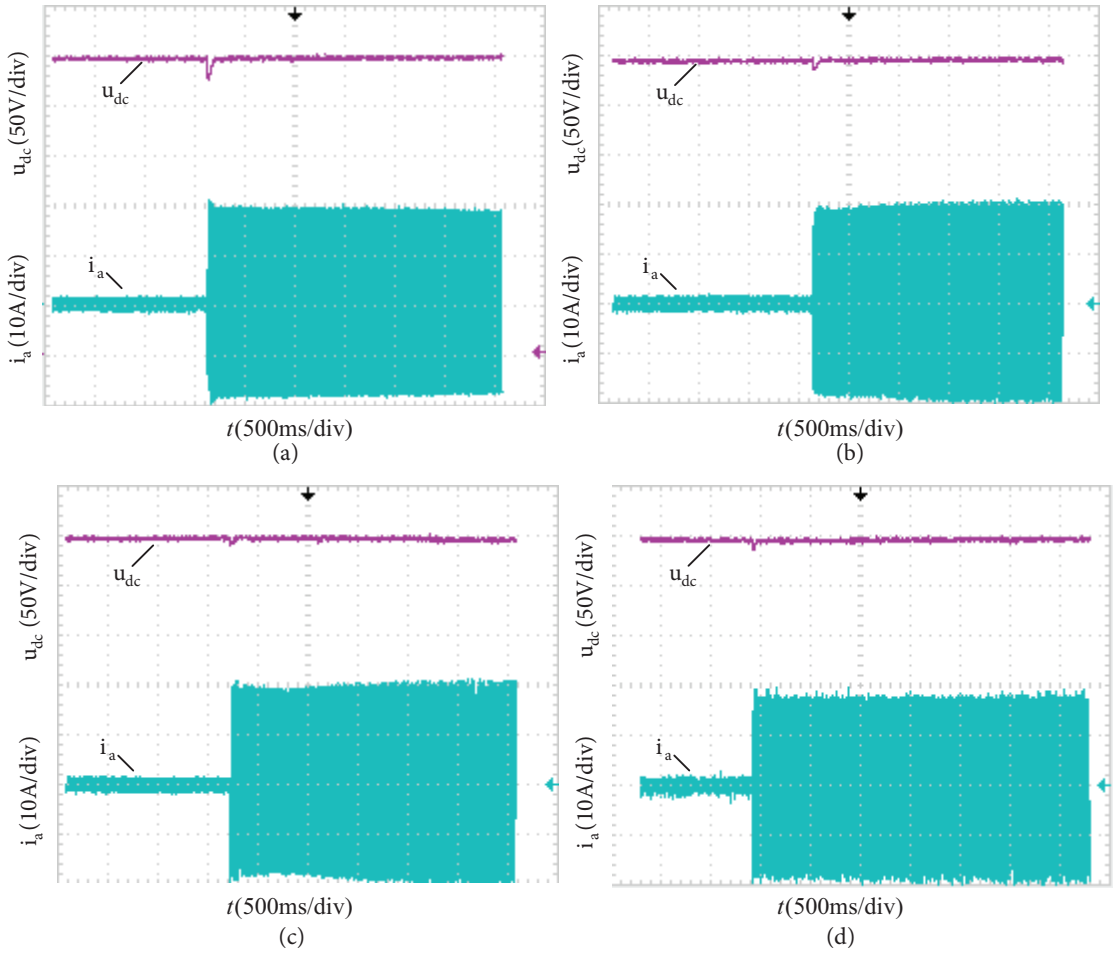

Figure 15. The diagram for response waveforms of three control strategies when DC-link loads mutate (approximately 0.1–2 kW): (a) under nonfeedforward control ($kp_2 = 5$ and $ki_2 = 157$); (b) under the traditional feedforward control ($kp_2 = 5$ and $ki_2 = 157$); (c) under two-step feedforward control ($kp_2 = 5$ and $ki_2 = 15700$); (d) under the traditional feedforward control ($kp_2 = 15$ and $ki_2 = 157$).

Figure 16 respectively shows the diagram of steady-state waveforms under three control strategies and the diagram of start-up waveform under two-step feedforward control, among which Figure 16a, 16b, 16c, and 16d respectively use the same parameters of current regulator as in Figure 15. Table 2 shows the performance comparison of the three control strategies. It can be seen that under nonfeedforward control, the quality of grid current is in the best state, but when the proportional coefficient of current regulator is taken as $kp_2 = 15$, the current waveform under the traditional feedforward control has a serious distortion. Though the amplitude of DC bus voltage dip is almost identical in Figures 15c and 15d, it can be seen that the current distortion increases significantly in Figure 16d. The current waveform under two-step feedforward control is basically consistent with that under the traditional feedforward control (both values of kp_2 are 5), and the waveform distortion rate is slightly higher than that under nonfeedforward control, which is mainly caused by the disturbance of grid voltage and DC bus voltage introduced by the feedforward branch. The second-step feedforward branch introduces a certain disturbance in addition; thus, under the two-step feedforward control, the rate of current waveform distortion slightly increases. Figure 16e shows the diagram for start-up waveform under two-step feedforward control with light loads. Table 3 shows start-up performance of the proposed strategy. It can be

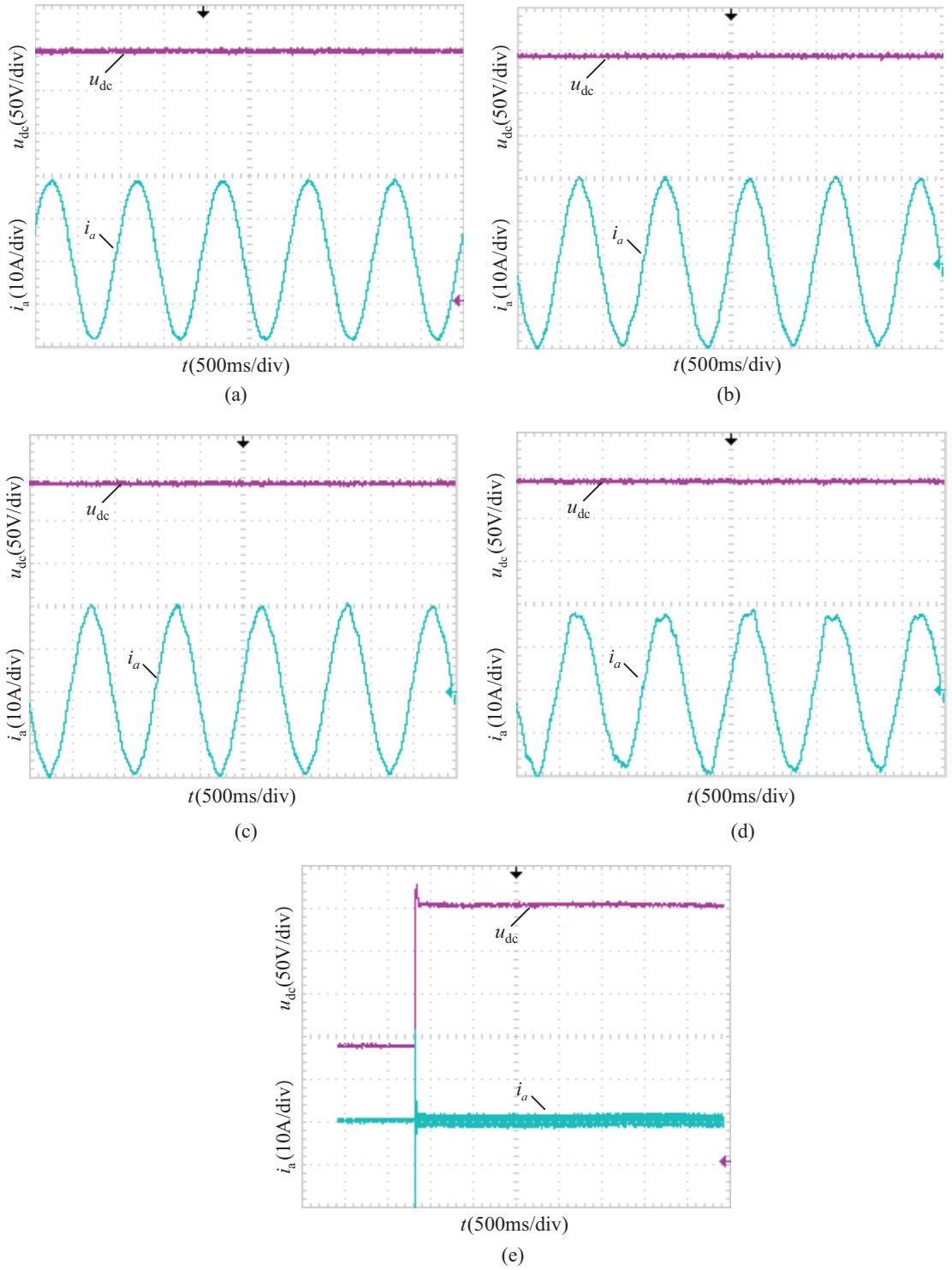

Figure 16. The diagram for steady-state waveform under the control of three control strategies and start-up waveform under two-step feedforward control: (a) under nonfeedforward control ($kp_2 = 5$ and $ki_2 = 157$); (b) under the traditional feedforward control ($kp_2 = 5$ and $ki_2 = 157$); (c) under two-step feedforward control ($kp_2 = 5$ and $ki_2 = 15700$); (d) under the traditional feedforward control ($kp_2 = 15$ and $ki_2 = 157$); (e) diagram for converter start-up under two-step feedforward control ($kp_2 = 5$ and $ki_2 = 15700$) with light loads.

seen that the DC bus voltage responds quickly. The rated current peak is 20 A as the limit. At start-up, grid current reaches the rated current peak rapidly and is controlled by the limit. The less overshoot can also verify the analysis of current loop characteristics in Figure 10 and show the controllability of the proposed strategy. The data in Tables 2 and 3 were gotten by data files (*.csv) that together with the waveforms used in this paper were saved from the oscilloscope.

Table 2. Performance comparison of three control strategies.

Control strategy	Voltage dip (V)	Settling time (ms)	THD of grid current (%)
Nonfeedforward control ($kp_2 = 5$ and $ki_2 = 157$)	24	80	3.24
Traditional feedforward control ($kp_2 = 5$ and $ki_2 = 157$)	12	82	3.94
Traditional feedforward control ($kp_2 = 15$ and $ki_2 = 157$)	10	38	6.15
Two-step feedforward control ($kp_2 = 5$ and $ki_2 = 15700$)	8	35	4.14

Table 3. Start-up performance of the proposed strategy.

	Overshoot	Settling time
Grid current	2 A (beyond the limit 20 A)	56 ms
DC bus voltage	26 V	80 ms

6. Conclusion

The energy feedback or absorption in the load side of the VSC needs two-step energy transmission, which passes the converter grid side and converter DC side, and then goes to the grid. When mutation happens, the contradiction of the current change in both sides of the converter is the main reason for DC bus voltage fluctuation. Furthermore, due to the irreconcilable contradiction, the DC bus voltage fluctuates inevitably. Besides some factors such as the time constant of inductance and DC-link capacitor, how to improve the response speed of control system is the key to reduce the fluctuation. The traditional feedforward control is restricted by the parameters of current regulator, so the response is relatively slow and the amplitude of the DC bus voltage fluctuation is larger. Therefore, this paper respectively proposes two feedforward branches to the given current and the given voltage in the d axis. Comparative analysis of three control strategies, i.e. nonfeedforward control, traditional feedforward control, and two-step feedforward control, shows that grid voltage mutation and DC-link load mutation have the same disturbance law for DC bus voltage under the three control strategies, and the difference between their gains is only b times. In addition, two-step feedforward control can improve the response speed of the voltage outer loop to reduce DC bus voltage fluctuation without losing the performance of the current inner loop. The experimental results have been presented to prove the correctness of small signal analysis and to verify the feasibility of the proposed strategy.

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References

[1] Suul JA, Luna A, Rodriguez P, Undeland T. Virtual-flux-based voltage-sensor-less power control for unbalanced grid conditions. IEEE T Power Electr 2012; 27: 4071–4087.

[2] Castilla M, Miret J, Camacho A, Matas J, de Vicuna LG. Reduction of current harmonic distortion in three-phase grid-connected photovoltaic inverters via resonant current control. IEEE T Power Electr 2013; 60: 1464–1472.

[3] Agorreta JL, Borrega M, Pez J, Marroyo L. Modeling and control of N-paralleled grid-connected inverters with LCL filter coupled due to grid impedance in PV plant. IEEE T Power Electr 2011; 26: 770–785.

[4] Teodorescu R, Liserre M, Rodriguez P. Grid Converters for Photovoltaic and Wind Power Systems. Singapore: John Wiley & Sons, 2011.

[5] Wan C, Huang M, Chi T, Wong S, Run X. Nonlinear behavior and instability in a three-phase boost rectifier connected to a nonideal power grid with an interacting load. IEEE T Power Electr 2013; 28: 3255–3265.

[6] Liu F, Duan S, Cha X. Design of two loop controller in gird-connected inverter with LCL filter. Proceedings of the CSEE 2009; 12: 234–240.

[7] Xu Z, Xu A, Xie S. Dual-loop grid current control technique for grid-connected inverter using an LCL filter. Proceedings of the CSEE 2009; 29: 36–41.

[8] Li S, Li Y, Chen RStudy of the optimum feed-forward control strategy in back-to-back converter system. Proceedings of the CSEE 2006; 25: 74–79.

[9] Li S, Li Y. Study of restraining DC-bus voltage fluctuation control strategy in back-to-back converter system. Electric Drive 2007; 37: 30–38.

[10] Zhao R, He Y, Liu Q. Research on improvement of anti-disturbance performance for three-phase VSCs. Transactions of China Electrotechnical Society 2004; 19: 67–72.

[11] Hur N, Jung J, Nam K. A fast dynamic DC-link power-balancing scheme for a VSC–inverter system. IEEE T Ind Appl 2001; 48: 794–803.

[12] Liu C, Xu D, Zhu N, Frede B, Chen M. DC-voltage fluctuation elimination through a DC-capacitor current control for DFIG converters under unbalanced grid voltage conditions. IEEE T Power Electr 2013; 28: 3206–3218.

[13] Lin J, Li G, Sun Y, Li X. Small signal analysis and control system parameter optimization for DFIG wind turbines. Automation of Electric Power Systems 2009; 33: 86–90.

[14] Qu B, Lu Z. Small-signal modeling and controller design of three-phase voltage source VSC. Transactions of China Electrotechnical Society 2010; 25: 103–108.

[15] Hu J, Zhu J, Dorrell DG, Guerrero JM. Virtual flux droop method – a new control strategy of inverters in microgrids. IEEE T Power Electr 2013; 99: 1–9.

[16] Figueres E, Garcerá G, Sandia J, Gonzalez-Espin F, Rubio JC. Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter. IEEE T Ind Appl 2009; 56: 706–711.

[17] Figueres E, Garcerá G, Sandia J, Gonzalez-Espin F, Rubio JC. Dynamic analysis of three-phase photovoltaic inverters with a high order grid filter. In: 2007 IEEE International Symposium on Industrial Electronics; 4–7 June 2007; Vigo, Spain. Piscataway, NJ, USA: IEEE. pp. 691–696.

[18] Bao X, Zhuo F, Tian Y, Tan P. Simplified feedback linearization control of three-phase photovoltaic inverter with an LCL filter. IEEE T Power Electr 2013; 28: 2739–2752.

[19] Liserre M, Blaabjerg F, Hansen S. Design and control of an LCL-filter based three-phase active converter. IEEE T Ind Appl 2005; 41: 1281–1291.