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Improving the SRF method to compensate low-order harmonics under nonsinusoidal network voltages

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Abstract: Increasing the application of power in electronic devices has increased the harmonics in power systems. Numerous methods like the synchronous reference frame (SRF) and the p-q-based method have been suggested to overcome the effects of these harmonics. The conventional SRF method provides acceptable results in harmonic compensation of high-order harmonics (higher than the fourth order), but the transient response time will be drastically increased in the presence of low-order harmonics due to the existence of a conventional low-pass filter. Furthermore, if the load terminal voltages are distorted, then the conventional SRF method will become unable to implement load current compensation. This research has used wavelet transform to overcome these difficulties. The proposed method is not only faster than conventional SRF, but it can also compensate the load currents if the load terminal voltages are also distorted. The simulation and experimental results are performed using MATLAB/Simulink and digital signal processor TMS320F28335 to verify the proposed method.

Key words: Active filter, digital signal processor, harmonic, synchronous reference frame, wavelet transform

1. Introduction

Harmonic distortion of power systems is a critical issue that has been investigated extensively. The existence of harmonics in power systems can cause some difficulties such as increasing power losses, decreasing maximum capacity of transmission lines, and interference with communication signals [1]. Numerous methods including the synchronous reference frame (SRF) and p-q-based method have been suggested to minimize these effects [2–5].

Among different harmonic compensation techniques [6], the SRF method has been extensively adopted for harmonic compensation [7,8]. This method usually employs a conventional second-order low-pass filter (LPF) to separate the DC component of the d-axis current. When there are low-order harmonics (i.e. of the second and third order) in the voltage/current of the power system, the transient response of this LPF will be prolonged, leading to an increased reaction time of the active power filter (APF). One other problem of the conventional SRF method is that load current compensation in the shunt APF will not be done if the load terminal voltages are distorted.

Some papers have proposed different solutions to resolve the drawbacks of the conventional SRF method. In [9], a modified phase-locked loop (PLL) structure was proposed to improve the total harmonic distortion

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(THD) of compensated current and voltage. In this paper, the compensated current THD was limited to 2.7% in the best case and transient response time was equal to 2 cycles. In [10], to improve the performance of APFs based on the SRF and the p-q methods under a nonsinusoidal load terminal voltages condition, a self-tuning filter was used. This method limited the compensated current THD to 2.07% in the best case. In [11], the performance of the SRF method was improved by neural networks under sinusoidal load terminal voltages, and the compensated current THD and transient response were limited to 1.45% and 1.5 cycles, respectively. In [12], a conventional LPF was replaced with a wavelet-based LPF in the p-q method to improve the time response of the APF. The suggested method improved the transient response time to 1 cycle under sinusoidal load terminal voltages while the effects of the mother wavelet were not studied.

In studies on improving the SRF method, improvements in transient response time and current compensation under nonsinusoidal load terminal voltages have not been considered together. In this paper, the conventional SRF method for shunt active power filters (SAPFs) has been modified so that the transient response time is improved and the current compensation is continued under nonsinusoidal load terminal voltages. For this purpose, a new wavelet-based method is proposed to generate the orthogonal signals under nonsinusoidal load terminal voltages and the conventional LPF is replaced with the wavelet-based LPF that was proposed in [12]. In both cases, the effects of different mother wavelets on the accuracy and the time response are studied. The proposed method has some advantages, such as a fast transient response (approximately 1 cycle) and load current compensation under the nonsinusoidal load terminal voltages. Moreover, the compensated current THD is also limited to 1.90% in the worst case.

In order to investigate the validity of the proposed method, a 3-phase power system is simulated in MATLAB and both experimental and simulation results are represented using MATLAB/Simulink and digital signal processor (DSP) TMS320F28335.

2. Wavelet transform

Wavelet transform (WT) is a time-frequency tool that can decompose the input signal to different frequency bands [13]. This transform has found many applications in power systems, such as harmonic detection and power calculation [14,15]. In the WT, a signal spectrum can be decomposed into nonoverlapping frequency bands. The WT of a continuous signal ($f(t)$) at a scale α and position τ is computed by Eq. (1) [16]:

$$W_f(\alpha,\tau) = |\alpha|^{-\frac{1}{2}} \int f(t)\Psi^*(\frac{t-\tau}{\alpha})dt, \tag{1}$$

where the symbol * denotes the complex conjugate and Ψ is the mother wavelet. The mother wavelet is a function of zero average and a limited period that is dilated with a scale parameter α and translated by τ:

$$\psi_{\alpha,\tau}(t) = |\alpha|^{-\frac{1}{2}} \psi(\frac{t-\tau}{\alpha}) \qquad \alpha,\tau \in R; \alpha \neq 0 \ . \tag{2}$$

The signal $f(t)$ can be decomposed by Eq. (3) [16]:

$$f(t) = \frac{1}{C_\psi} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{1}{\alpha^2} W_f(\alpha,\tau)\psi(\frac{t-\tau}{\alpha})d\alpha d\tau, \tag{3}$$

where $C_\psi = \int_{-\infty}^{\infty} \frac{|\psi(\omega)|^2}{\omega} d\omega < \infty$.

There are 3 methods to implement the discrete wavelet transform (DWT). These are multiresolution analysis (MRA), windowed wavelet transform (WWT), and lifting wavelet transform (LWT), which will be introduced in the next subsections.

2.1. Multiresolution analysis

In 1989, Mallat introduced MRA in wavelet theory for the implementation of the DWT and unified the structure of the wavelet orthogonal basis. He proposed that discrete signals could be decomposed and restructured according to the WT [17]. MRA involves a high-pass finite impulse response (FIR) filter ($g(z)$), a low-pass FIR filter ($h(z)$), and downsampling. The FIR filter coefficients are determined by the mother wavelet.

In the MRA, the input signal is passed through high-pass and low-pass filters and then is downsampled by 2. This process decomposes the input signal into detail and approximation components, which consist of high- and low-frequency components, respectively. Figure 1 shows the one-level MRA structure. For increasing the MRA levels, several series of Figure 1 are used.

In MRA, the relationship between sampling frequency (f_s) and the upper limit of the lowest frequency band (f_u) can be written as in Eq. (4) [12,18]:

$$f_u = \frac{f_s}{2^{N+1}}, \tag{4}$$

where N is the number of MRA levels.

2.2. Windowed wavelet transform

WWT is the same as MRA, but in this method, the input signal must be windowed as a multiple of 2^N, where N is the number of wavelet levels.

2.3. Lifting wavelet transform

In MRA, the input signal is passed through low-pass and high-pass filters and then is downsampled by 2. In other words, all of the data are analyzed first, and then half is removed. For decreasing the computational cost in the LWT, the input signal is first downsampled by 2, and then analyzed by predicts and updates. The structure of LWT for 1 prediction and 1 update is shown in Figure 2 (unnormalized). In this figure, $t_1(z)$ and $s_1(z)$ are Laurent polynomials.

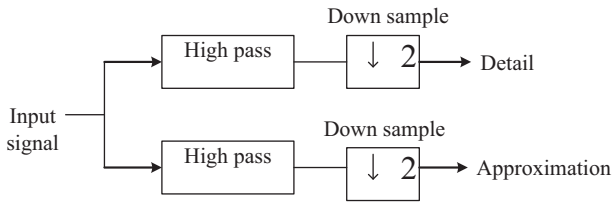

Figure 1. Multiresolution analysis.

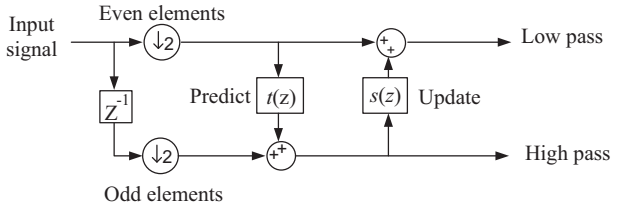

Figure 2. Structure of LWT for 1 prediction and 1 update.

Any finite length filter such as $h(z)$ can be written in polyphase form as below [19]:

$$h(z) = h_e(z^2) + z^{-1}h_o(z^2), \tag{5}$$

where $h_e(z^2)$ is the even sequence, $h_o(z^2)$ is the odd sequence, and z^{-1} is the delay unit that indicates the delay between an even and odd sequence. The polyphase matrix for pair of complementary filters (h and g) can be written as in Eq. (6) [18]:

$$P(z) = \begin{bmatrix} h_e(z) & g_e(z) \\ h_o(z) & g_o(z) \end{bmatrix}. \tag{6}$$

In [19], it was shown that the polyphase matrix ($P(z)$) can be decomposed as in Eq. (7) and the decomposition of $P(z)$ is continued until a matrix remains with only 2 constants on its main diagonal.

$$P(z) = \prod_{i=1}^{m} \begin{bmatrix} 1 & s_i(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ t_i(z) & 1 \end{bmatrix} \begin{bmatrix} k & 0 \\ 0 & \frac{1}{k} \end{bmatrix} \tag{7}$$

In the LWT, the whole transform can be done in place, without using any auxiliary memory. Moreover, the transferred data take the same place as the input data [20]. In [21], it was proven that for filters of long length, the LWT leads to a decrease in the computation complexity by half with respect to the conventional FIR filter banks that are used in MRA and WWT.

3. Synchronous reference frame method

The application of SRF for harmonics compensation was introduced in [22]. The current signal is transferred to the d-q coordinate by Park transform (Eq. (8)) in this method. The amount of main frequency in the d-q coordinate appears as a DC value while the other harmonics emerge as an AC value. In other words, all frequencies are decreased by a specific amount. After that, the amount of the DC component of the d-axis is separated by LPF and subtracted from the original signal. As a result, only the AC component, which is proportional to the load current harmonics, will remain. Afterwards, the AC component will be returned to the abc coordinate by an inverse Park transform in order to yield a reference current. Figure 3 depicts the conventional SRF method.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta - \frac{4\pi}{3}) \\ sin\theta & sin(\theta - \frac{2\pi}{3}) & sin(\theta - \frac{4\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{8}$$

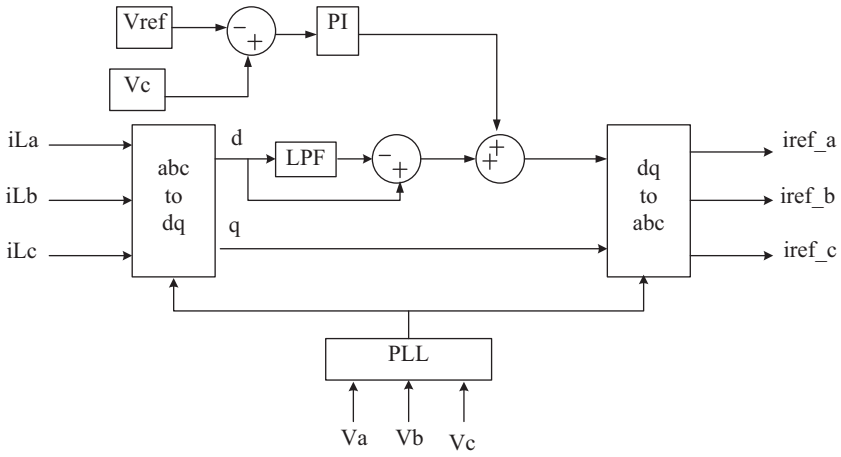

Figure 3. Conventional SRF method.

4. Proposed method

As mentioned, the conventional SRF method has some drawbacks. This method is unable to compensate the load currents under the distorted load terminal voltages and the transient response time will be increased when there are low-order harmonics in the load currents. In the proposed method to solve existing drawbacks, the typical LPF and PLL are replaced with the wavelet-based LPF that was designed in [12] and a block to produce orthogonal signals, respectively. The block diagram of the suggested method is shown in Figure 4. The MATLAB simulation blocks are shown in Figure 5.

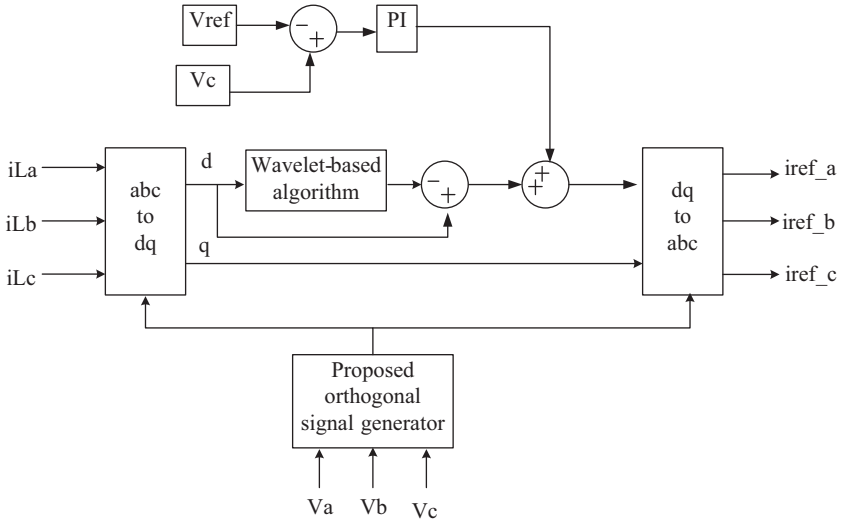

Figure 4. Proposed method: block diagram.

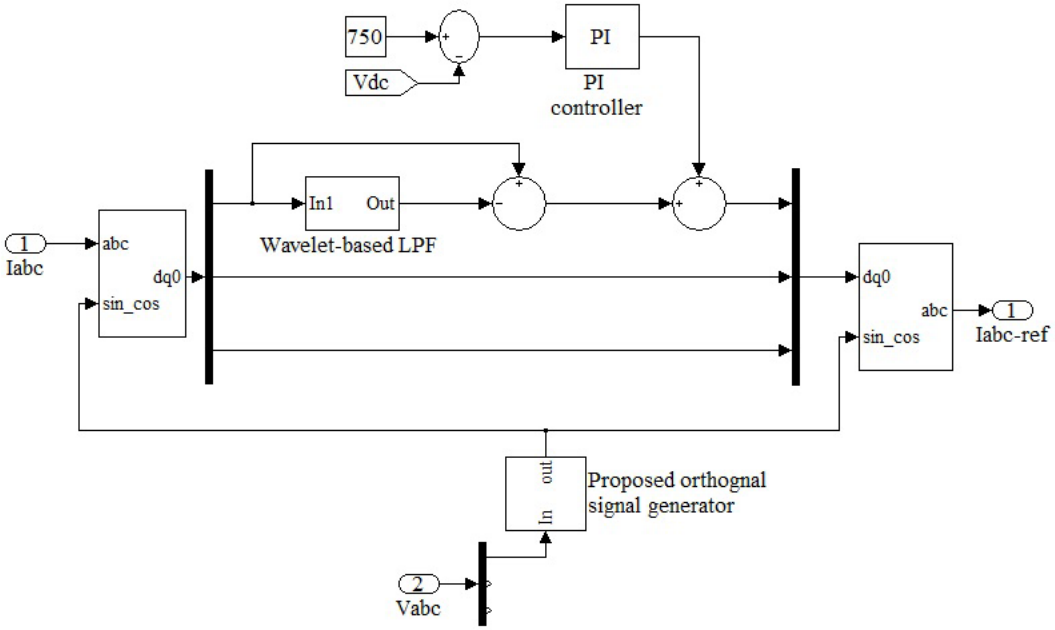

Figure 5. Proposed method: MATLAB simulation blocks.

In the wavelet-based LPF, the d-axis current is decomposed by WT to various frequency bands, and the lowest range that contains only the DC component is chosen. After that, this value is subtracted from the

original signal to yield the AC component. Extracting the frequency bands of a signal using WT depends on the mother wavelet and sampling frequency. These 2 important factors may lead to a longer response time of the WT or reduced accuracy of frequency bands extracted when chosen incorrectly. The sampling frequency determines the number of WT levels in accordance with Eq. (4). Meanwhile, more complex mother wavelets must be used in order to have more accurate frequency bands. As the mother wavelet is more complex, the calculations take more time and thus there will be longer delays.

The proposed orthogonal signal generator contains 4 parts. The first part is a DWT and an inverse discrete wavelet transform (IDWT) for the extraction of the fundamental [23], the second is a method for orthogonal signal generating that was introduced in [24], the third is the conversion of a Cartesian coordinate to a polar coordinate, and the fourth is the phase correction part. The structure of the proposed orthogonal signal generator is illustrated in Figure 6, and its MATLAB simulation blocks are shown in Figure 7, where n is a positive integer number, φ is a constant number in rad that is used for phase correction, and only the load terminal voltage of phase a (Va) is used for fundamental component extraction by the WT.

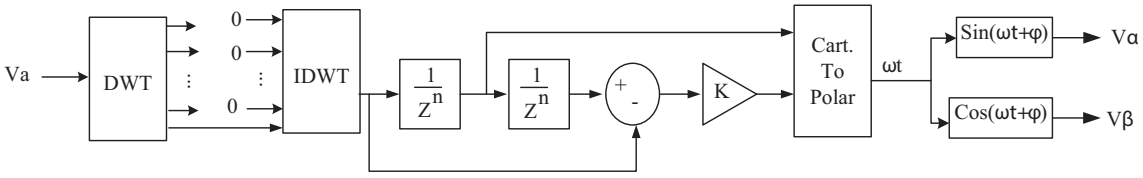

Figure 6. Proposed orthogonal signal generator.

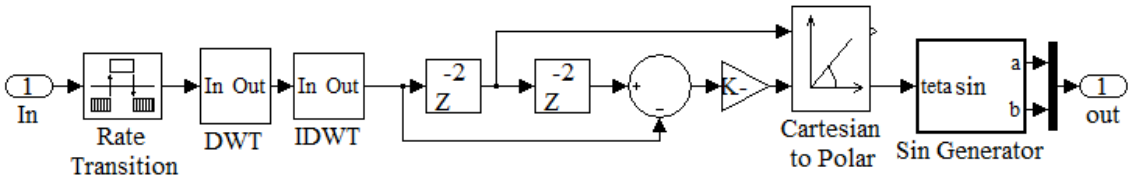

Figure 7. Proposed orthogonal signal generator MATLAB simulation blocks.

5. Simulation results

The power system depicted in Figure 8 will be simulated in MATLAB for the comparison of conventional SRF and the proposed method. This power system is equipped with a diode rectifier and a hypothetical load. The hypothetical load generates second and third harmonics in addition to containing the fundamental component. The diode load is also able to be connected/disconnected to the network at any time. The voltages of this network have third and fifth harmonics, which are shown in Figure 9. Additional features of the power system can be found in the Appendix.

5.1. Wavelet level determination

In order to find the number of wavelet levels, one must specify the existing harmonics in the input signal. In the proposed method, the signal decomposition using WT is done in 2 blocks. These are wavelet-based LPF and the proposed orthogonal signal generator. To specify the number of wavelet-level decompositions in the wavelet-based LPF block, the load currents and their frequency analysis using FFT are depicted in Figures 10 and 11. As can be seen in Figure 11, the lowest-order harmonic available in the load currents is the second harmonic. Therefore, the current of the d-axis will have a frequency of 50 Hz. With respect to Eq. (4) for

finding the amount of the DC component of the d-axis current, if the current is sampled at 1600 Hz, then 5 decomposition levels will be required to achieve a frequency band of 0–25 Hz, which contains only the DC component.

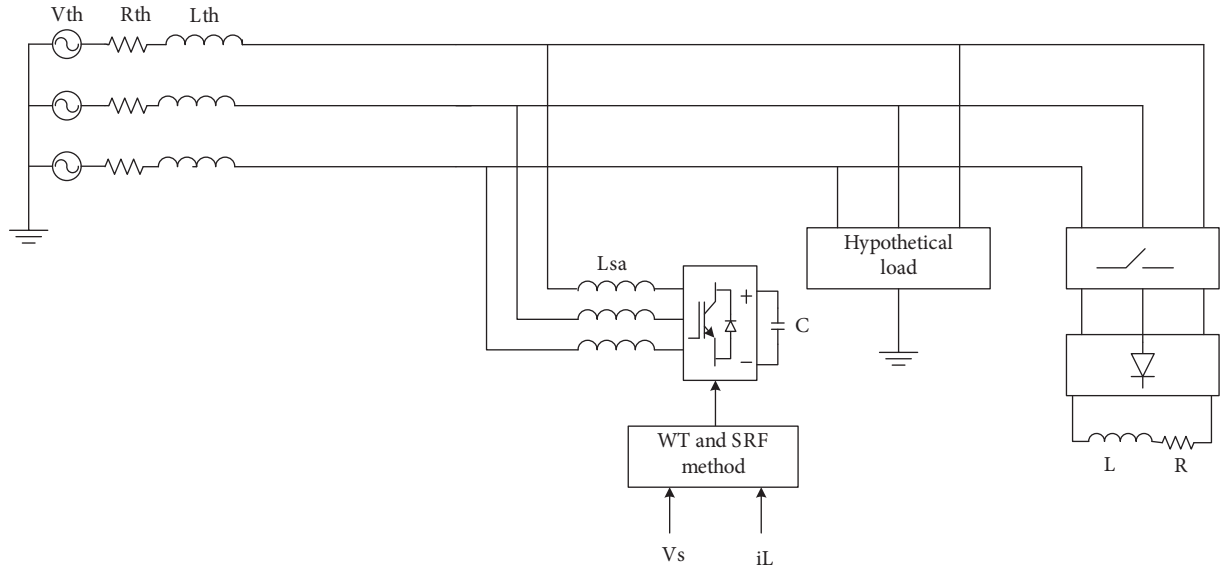

Figure 8. Studied network.

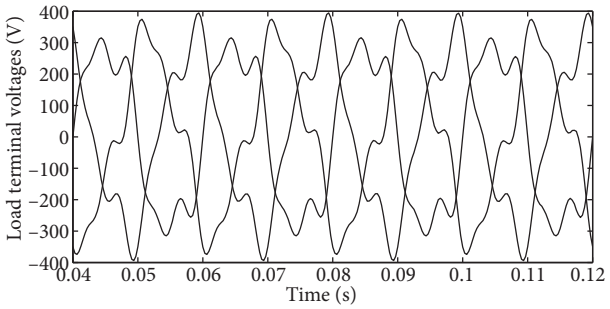

Figure 9. Load terminal voltages.

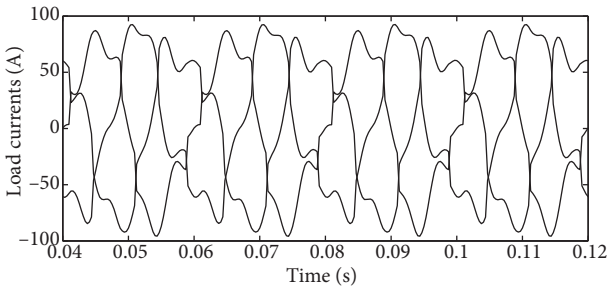

Figure 10. Load currents under a distorted condition.

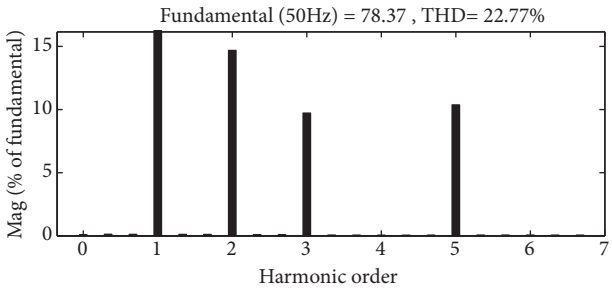

Figure 11. Frequency spectrum of load currents under a distorted condition.

As mentioned before, the load terminal voltages contain third- and fifth-order harmonics. Therefore, according to Eq. (4), if the load terminal voltage is sampled at 1600 Hz, then 3 decomposition levels will be

required in the proposed orthogonal signal generator block to achieve a frequency band of 0–100 Hz, which contains only fundamental components (50 Hz). In the next sections, the abovementioned wavelet levels and sampling frequency will be used in the wavelet-based LPF and proposed orthogonal signal generator blocks.

5.2. Effects of mother wavelet

As mentioned in earlier sections, the LWT has some advantages over MRA and WWT (such as low computational cost). Moreover, in [12], the 3 abovementioned wavelet methods were compared and the LWT was proposed for WT implementations. As a result, in our study, the LWT will be used for the implementation of DWT, and the effects of mother wavelets are examined in the next subsections.

5.2.1. Effects of the mother wavelet on wavelet-based LPF

As mentioned before, one of the most important factors in wavelet analysis is the mother wavelet. To select the best mother wavelet in DC component extraction of a d-axis current, this term of current, shown in Figure 12, is decomposed by 4 different mother wavelets and the results are shown in Figure 13. Additionally, the amount of delay time that is created by each mother wavelet is listed in Table 1. According to Figure 13 and Table 1, the delay time caused by the Haar mother wavelet is less than other mother wavelets and this is the best choice for the extraction of the DC component of the d-axis current.

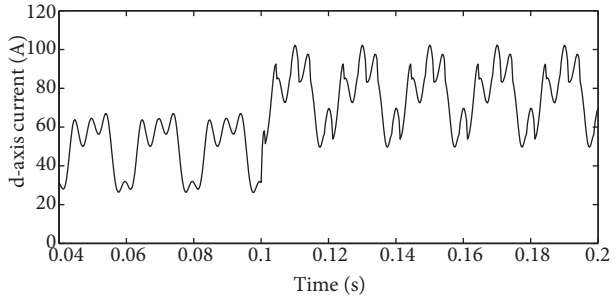

Figure 12. The d-axis current under distorted load terminal voltages and current.

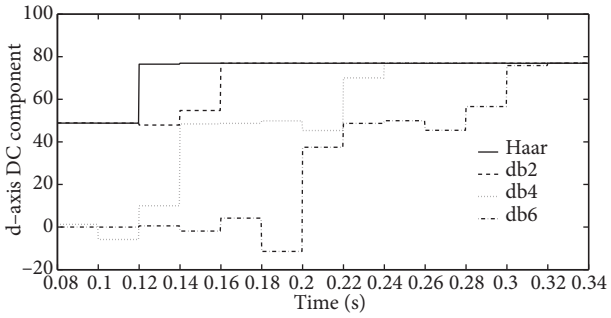

Figure 13. Extracted DC component of d-axis by 4 different mother wavelets.

Table 1. Delay caused by 4 different mother wavelets.

Mother wavelet	Haar	db2	db4	db6
Delay (ms)	20	60	140	200

5.2.2. Effects of the mother wavelet on the proposed orthogonal signal generator

In the proposed orthogonal signals generator, the fundamental voltage is extracted by the DWT and IDWT. As mentioned before, the Haar mother wavelet has the best performance in the DWT in terms of the response time. To choose the best mother wavelet for IDWT, the reconstructed fundamental voltage of phase a by different mother wavelets is shown in Figure 14 and their THDs are listed in Table 2. According to Figure 14 and Table 2, the db8 mother wavelet has an acceptable performance in terms of the THD value of the output signal and is chosen for fundamental reconstruction of the load terminal voltage.

Table 2. THD of extracted fundamental of load terminal voltage of phase a by different mother wavelets.

Mother wavelet	Haar	db3	db5	db6	db8
THD (%)	48.24	16.15	7.14	4.85	2.28

5.3. Load currents compensation

The load currents are increased at t = 0.1 s to investigate the performance of the conventional SRF and the proposed method at different load variations. Load terminal voltages are the same as those in Figure 9 and the load currents are shown in Figure 15. The load currents' THD before and after a load increase is equal to 40.43% and 26.92%, respectively.

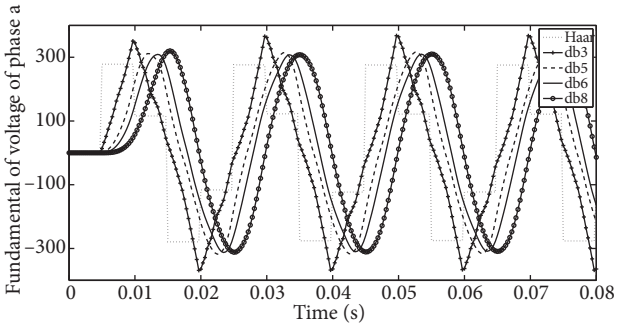

Figure 14. Extracted fundamental of load terminal voltage of phase a by different mother wavelets.

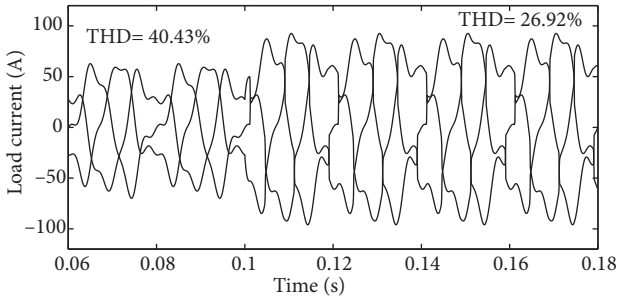

Figure 15. Load currents.

Figures 16 and 17 represent 3 phase currents after compensation by the 2 abovementioned methods. The compensated current using the proposed method responds suddenly after 1 cycle and follows the new amplitude, whereas the conventional SRF method cannot compensate the load currents under the distorted source voltage condition. The compensated currents' THD before and after the load increase is equal to 1.64% and 1.90%, respectively.

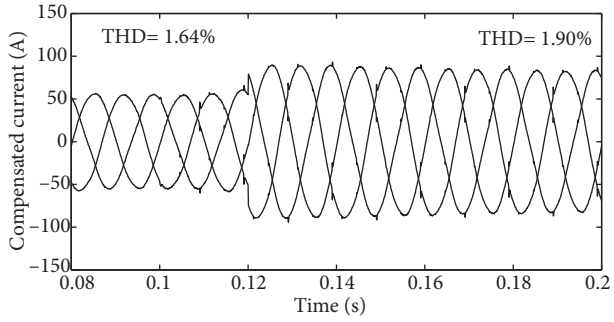

Figure 16. Compensated current by the proposed method.

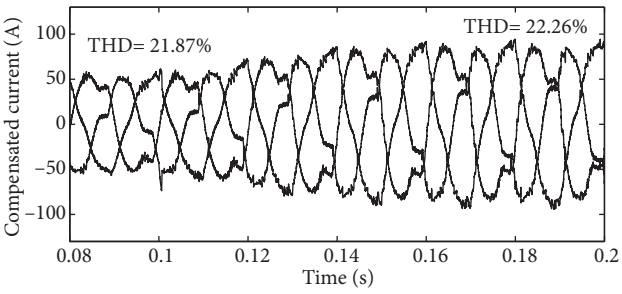

Figure 17. Compensated current by the conventional SRF method.

In Figure 18, the compensation current of an active power filter for phase a is shown. As can be seen, the compensation current of the active power filter is also increased after connecting the diode rectifier load.

The compensated current of phase a is illustrated in Figure 19 for both methods to study the SAPF response more accurately. It can be noted that the response of the SAPF reaches the desired value after 20 ms using the proposed method, while the conventional SRF method has not only failed to perform compensation

but has also increased the SAPF delay time to 40 ms. This delay time is the same as the delay time that was presented in [25].

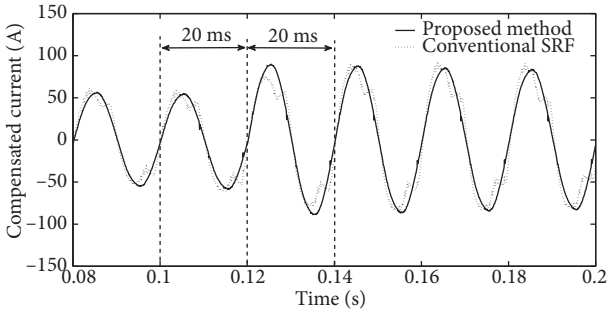

Figure 18. Compensation current of active power filter for phase a.

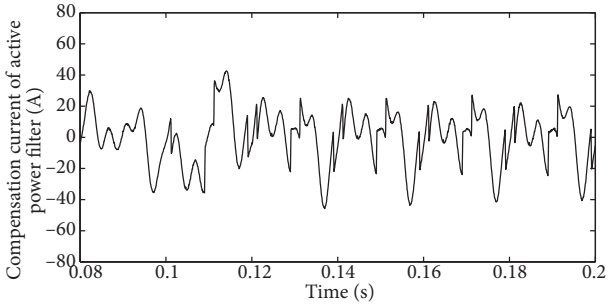

Figure 19. Compensated current of phase a under both methods.

DC link voltage variation under a load change condition is illustrated in Figure 20. The DC link voltage is dropped first and then increased to the set point value (750 V).

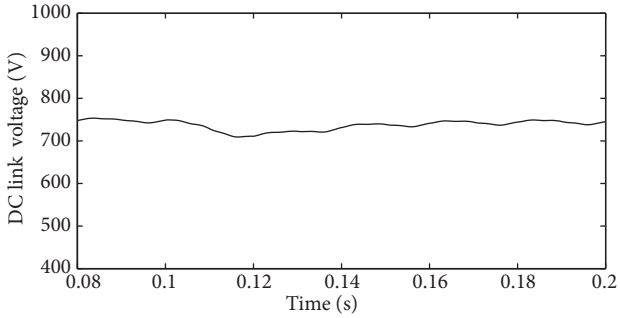

Figure 20. DC link voltage.

The disability of load compensation using the conventional SRF method under the distorted condition of load terminal voltages can be attributed to the PLLs, which have been utilized in this method for the production of orthogonal signals [9]. Orthogonal signals generated by conventional PLL and the proposed method are compared in Figure 21. It can be seen that the generated signals are distorted for the conventional PLL, which prevents the SAPF from performing compensation under nonsinusoidal load terminal voltages, but the proposed method has produced distortion-free orthogonal signals. The voltage signal of phase a was sampled at 1600 Hz in the proposed method and 3 decomposition levels with a Haar mother wavelet and 5 levels of signal reconstruction with a db8 mother wavelet were utilized in DWT and IDWT, respectively.

6. Experimental results

For the evaluation of the proposed method, the desired codes were generated by MATLAB and then loaded into DSP TMS320F28335 through a USB port as a real-time data exchange (RTDX). Figure 22 demonstrates how the DSP and PC are connected using RTDX. For experimental analyses, the desired signals are sent to the DSP through RTDX using MATLAB, and then they are sampled by the DSP at the frequency of 1600 Hz.

The extracted DC component of the d-axis current by different mother wavelets that were analyzed by the DSP is shown in Figure 23. Figures 13 and 23 show that the simulation and experimental results are almost

the same, except for the delay time of following the new amplitude, where the delay obtained from the DSP is 0.6 ms longer than that of the simulation and is equal to the sample time (1/1600 = 0.6 ms).

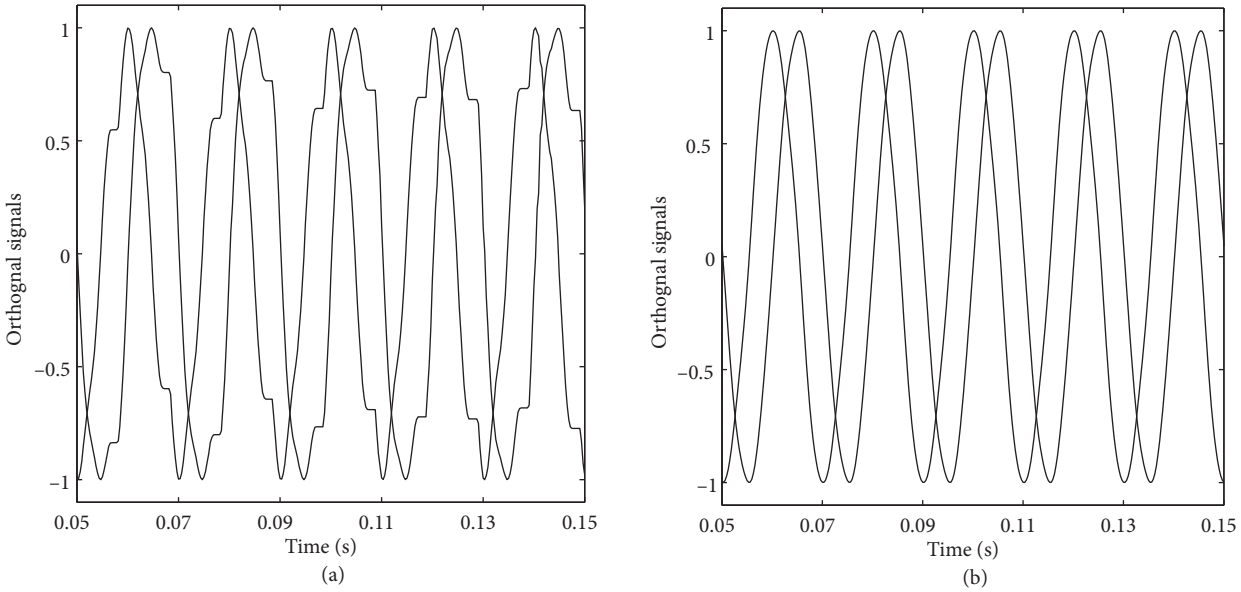

Figure 21. Orthogonal signals generated under distorted load terminal voltages: (a) conventional PLL; (b) proposed orthogonal signal generator.

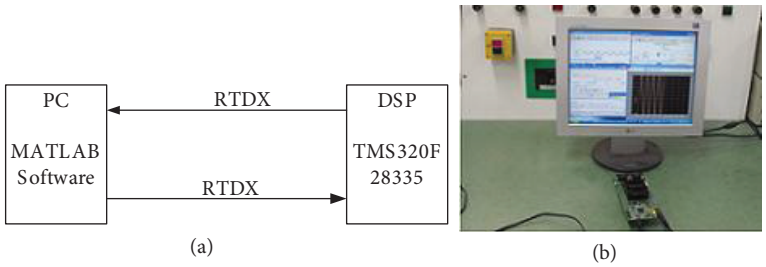

Figure 22. Hardware configuration between MATLAB and DSP: (a) schematic configuration; (b) experimental configuration.

For experimental analyses of the mother wavelet's effects in IDWT, the signal shown in Figure 10 is sent to the DSP through RTDX using MATLAB, and then it is reconstructed by different mother wavelets in the DSP. As in the simulation results, the decomposition is done by a Haar mother wavelet. The results obtained by the DSP for this study are shown in Figure 24. The difference between the simulation and experimental results is the same as before.

To investigate the performance of the proposed orthogonal signal generator by DSP, the voltage signal of phase a is sent to the DSP through RTDX and the conditions are the same as in the simulation. The output of the DSP is shown in Figure 25. As in the simulation results, the conventional PLL provides distorted orthogonal signals.

To compare the simulation and experimental results in detail, the fundamental of phase a and the DC component of the d-axis current that was obtained by the simulation and the experiment are shown in Figure 26. The results obtained from the simulation and the experiment are the same except for the delay time of 0.6 ms that exists in the experimental results. This is due to the inability of MATLAB to generate the optimal

DSP codes for the rate transition block that is applied to equate the input and output sampling frequency of the DSP.

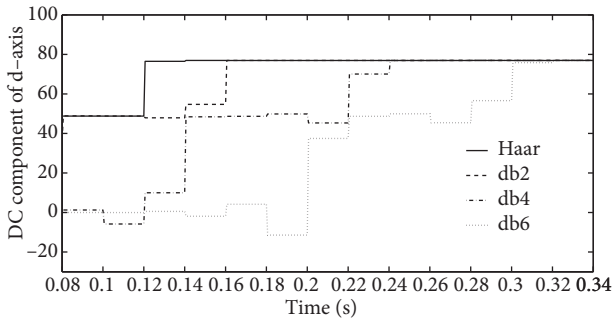

Figure 23. Effects of different mother wavelets on the signal decomposition (DSP output with f_s = 1600 Hz).

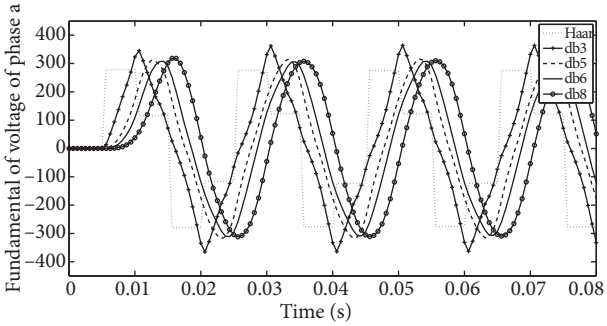

Figure 24. Effects of different mother wavelets on the signal reconstruction (DSP output with fs = 1600 Hz).

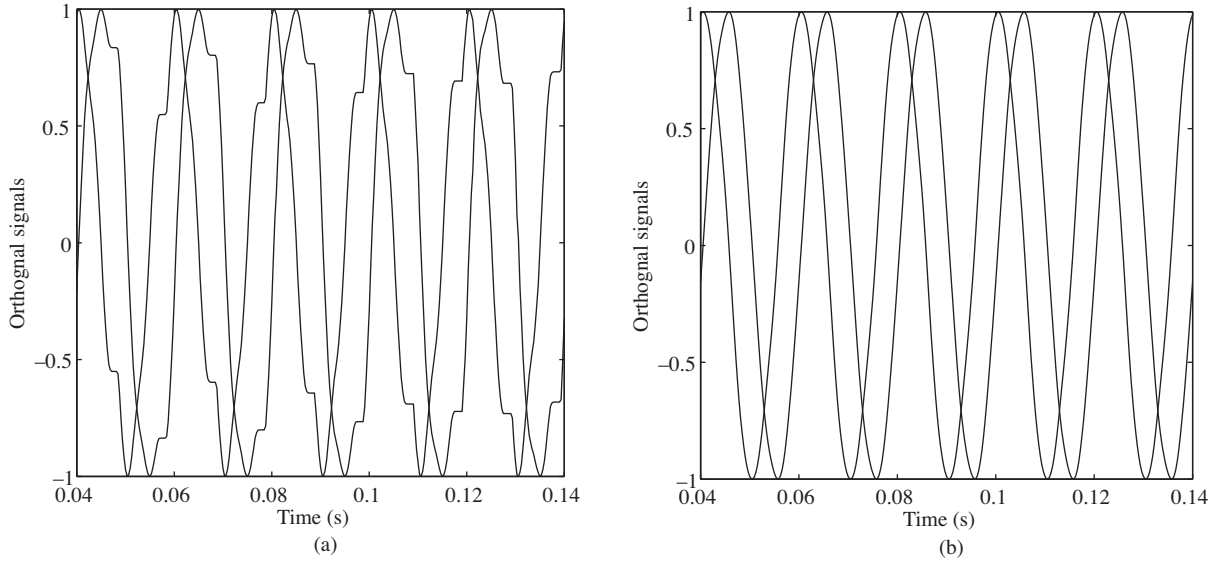

Figure 25. Orthogonal signals generated by DSP with 2 methods: (a) conventional PLL; (b) proposed orthogonal signal generator.

6.1. Discussion about sampling frequencies

The sampling frequency of reference currents must be high enough in practice to increase the accuracy of switching. In this paper, the d-axis current and phase a of voltage are sampled at 1600 Hz in wavelet-based LPF and the proposed orthogonal signal generator, respectively. The output of the wavelet-based LPF block is a DC value. In the decomposition process of the d-axis current by WT, the sampling frequency of the extracted DC value is decreased to 25 Hz by WT due to the downsampling that is performed in the WT. As is clear, this sampling frequency (25 Hz) is very low. A rate transfer block can be used to increase the sampling frequency of the DC value in practice. The rate transfer block does not make any error because the increased sampling frequency signal is a DC signal. However, in the simulation mode, MATLAB increases the sampling frequency of the extracted d-axis DC value to the required sampling frequency. This process is done automatically in the next block that the DC value passes through.

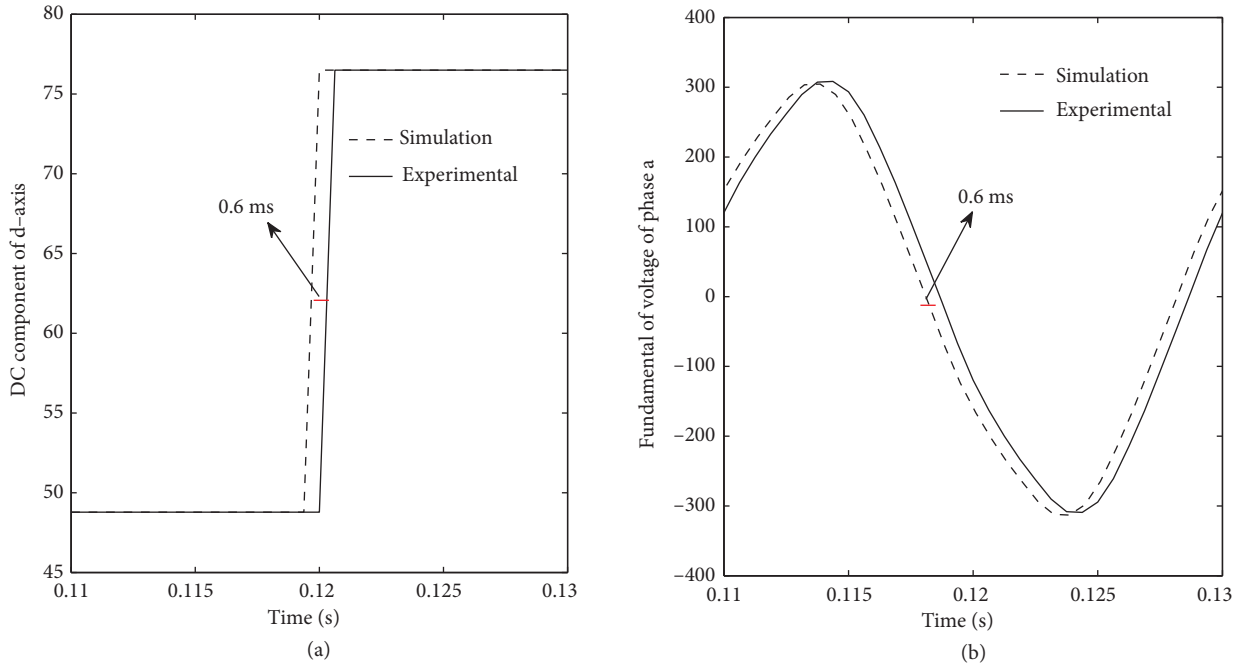

Figure 26. The difference between simulation and experimental results: (a) DC component of the d-axis; (b) fundamental of voltage of phase a.

In Figure 5, phase a of voltage is sampled at 1600 Hz and then the 3-level wavelet decomposition decreases the sampling frequency of the fundamental of phase a voltage to 100 Hz (this process is done in the DWT block of Figure 5). After that, the extracted signal is reconstructed by 5 levels to increase the accuracy of the extracted signal. In the reconstruction process, the sampling frequency is increased to 6400 Hz by upsampling. To further increase the sampling frequency, a rate transfer block can be used in practice as before. Because of the relatively high sampling frequency of the extracted signal (6400 Hz), the rate transfer block produces a very small error.

According to the abovementioned reasons, the sampling frequency of extracted signals can be increased to the desired sampling frequency without any significant error. Therefore, the reference currents can be calculated at the desired sampling frequency in practice.

7. Conclusions

Two important factors in SAPFs are transient response and the ability of compensation under nonsinusoidal load terminal voltages. In this paper, transient response time improvement and current compensation under nonsinusoidal load terminal voltages were considered together. For this purpose, the conventional LPF and PLL were replaced with wavelet-based LPF and a new orthogonal signal generator based on WT, respectively. The proposed method improves the APF transient response to 1 cycle and compensates the load currents under nonsinusoidal load terminal voltages. Moreover, the compensated current THD is limited to 1.90% in the worst case.

The proposed method was verified using both simulation and experimental results, and finally it was demonstrated that the experimental and simulation results were the same, except for the delay time of 0.6 ms that is equal to the sample time ($1/1600 = 0.6$ ms).

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Appendix

This appendix illustrates the parameters that are used in the simulations as shown in Figures 4, 5, and 6. The network data are given in Table 3.

Table 3. Network data.

R	L	C	L_{sa}	Vth (phase-to-phase RMS voltage)	Frequency	R_{th}	L_{th}	ω
20 Ω	10 mH	8 mF	0.5 mH	380 V	50 Hz	8 mΩ	1 μH	100 π

Table 4 shows the hypothetical load parameters under the first, second, and third harmonics. Table 5 demonstrates the second-order and PI parameters used in simulations.

V_{ref} = 750 V, n = 2, φ = 0.1 rad.

Table 4. Hypothetical load.

Fundamental	P	20 KW	Second harmonic	Vth	1400 V	Third harmonic	Vth	1400 V
	Q	100 Var		Rth	100 Ω		Rth	100 Ω

Table 5. PI and 2^{nd} order LPF parameters.

PI parameters	K_p	0.25	Second-order	Cut-off frequency	10 Hz
	K_i	1	LPF parameters	Damping factor	0.8