

1-1-2016

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SANKARARAJU, MANJULA and DHARMAR, SELVATHI (2016) "Design of low power CMOS LC VCO for direct conversion transceiver," *Turkish Journal of Electrical Engineering and Computer Sciences*: Vol. 24: No. 4, Article 85. <https://doi.org/10.3906/elk-1407-24>
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Design of low power CMOS LC VCO for direct conversion transceiver

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Received: 03.07.2014

Accepted/Published Online: 03.04.2015

Final Version: 15.04.2016

Abstract: A low power 1.2 GHz LC differential voltage-controlled oscillator (VCO) is designed for a direct conversion transceiver in 130 nm CMOS processes. It consists of a complementary current reuse structure and LC tank circuit. To produce a good tuning range and reduce losses in the tank circuit, modified inversion mode PMOS varactors and an on-chip inductor are designed with a better quality factor. The flicker noise is reduced by the PMOS tail current source connected in parallel with the capacitance. The 1.2 GHz LC VCO achieves a phase noise value of -132 dBc/Hz at 1 MHz offset and the tuning range of the oscillator is from 1.128 to 1.27 GHz for the control voltage, tuning from 0 to 1.5 V. It dissipates 245μ W power at 0.8 V supply voltage and the figure of merit is calculated as -199.7 dBc/Hz.

Key words: Phase noise, IMOS varactor, on-chip inductor, voltage-controlled oscillator

1. Introduction

The CMOS direct conversion transceiver (DCT) has gained widespread attention for low power applications due to the combined advantages of its simple architecture and easy integration with low power consumption and low cost. Important drawbacks of the DCT are the DC offset problem from self-mixing in the receiver side and injection locking in the transmitter side [1,2]. To eliminate these drawbacks, the frequency of the local oscillator is far away from the RF frequency. A voltage-controlled oscillator (VCO) acts as a local oscillator for up-conversion and down-conversion in the DCT and receiver. In this paper, a low power 1.2 GHz LC VCO is to be designed.

Figure 1 shows the general concept of the LC VCO. The inductor (L) and capacitor (C) are connected in parallel to form a resonator tank circuit, which produces oscillations with the loss of tank circuit g_{tank} .

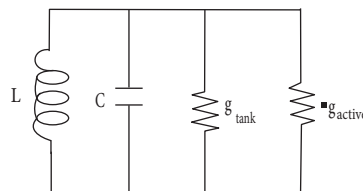


Figure 1. LC VCO concept.

To overcome the losses in the tank circuit, a negative conductance of the active devices g_{active} is added. Usually the cross-coupled structure of active devices produces negative conductance. Based on this concept, the conventional LC VCO, which consists of an NMOS cross-coupled pair with LC tank circuit, was designed [3].

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For low power consumption, many designers have approached the complementary current reuse structure for the LC VCO because this structure consumes half the amount of power of the conventional LC VCO [4–6]. In [7], a low power VCO was designed in 0.18 μm CMOS processes. It consisted of two optimized inductors and junction varactors of the NMOS differential pair. It dissipated 1.8 mW power. For improving the performance and reducing the power, a low voltage adaptive body bias LC VCO was presented, in which body bias was used to reduce the threshold voltage as well as back gate capacitances of NMOS transistors used for tuning purposes [8]. It achieved good figure of merit (FOM) and consumed 0.94 mW power at 0.4 V supply voltage, but only 6% of the tuning range was achieved.

Fiorelli et al. [9] analyzed different inversion regions based on g_m/I_d for an LC VCO design using 90 nm CMOS technology. The differential LC VCO was designed in the moderate inversion region, consumed 440 μA at a 1.2 V supply voltage, and produced 106.2 dBc/Hz phase noise at 400 kHz offset from the carrier. Zhou et al. proposed a low power low phase noise LC VCO in which an adaptive body biasing technique was used to reduce the PVT variation effect. The circuit drew 1.55 mA from a 1.5 V supply voltage [10]. Yu presented a low voltage low power LC VCO [11]. Forward body bias and admittance transforming techniques were adopted for low voltage. A voltage boosting circuit was used for widening the tuning range. The simulated LC VCO produced 39.3% tuning range at low power consumption of 562 μW . In this work, a low power low phase noise LC VCO is presented.

Usually, the CMOS LC-VCO has the following drawbacks: 1) monolithic inductor with poor quality factor, 2) tuning range of the varactors is very limited, and 3) flicker noise in CMOS is poorer. For eliminating these drawbacks, a low power complementary LC VCO with less phase noise and with PMOS tail current source is proposed in this paper. An on-chip planar spiral inductor with good quality factor and MOS varactors are designed. Section 2 describes the proposed LC VCO with LC tank circuit. Section 3 discusses the results and conclusions are described in Section 4.

2. VCO circuit

The proposed LC VCO is shown in Figure 2. It has a complementary cross-coupled differential pair with integrated LC tank. The cross-coupled connections of NMOSFETs (M1 and M2) and PMOSFETs (M3 and M4) are provided to meet the needed negative feedback and increase VCO transconductance while drawing the same quiescent drain current. For NMOS transistors, self-bias resistances (R_{Bias}) provide the appropriate bias points for M1 and M2 from differential output voltages. These resistances provide the diode connection of the switching transistors in DC while providing an opening in AC operation. They also protect the gates of MOS transistors and support low power operation. C1 and C2 are the coupling capacitors. The PMOS devices achieve better symmetry on each of the resonator nodes. For the complementary cross-coupled differential pair, the startup condition is written as:

$$\frac{1}{g_{tank}} = R_{tank} \geq \left(\frac{2}{g_{mNMOS}} // \frac{2}{g_{mPMOS}} \right) \quad (1)$$

where g_{mNMOS} and g_{mPMOS} are the transconductances of the cross-coupled pair of NMOSFETs and PMOSFETs, respectively. R_{tank} is the parallel loss of the tank circuit. The negative conductances of the active circuit compensate the loss of the tank circuit.

The LC tank circuit, which consists of MOS varactors and an on-chip spiral inductor, is designed to produce a good tuning range, which will be discussed in the following subsections.

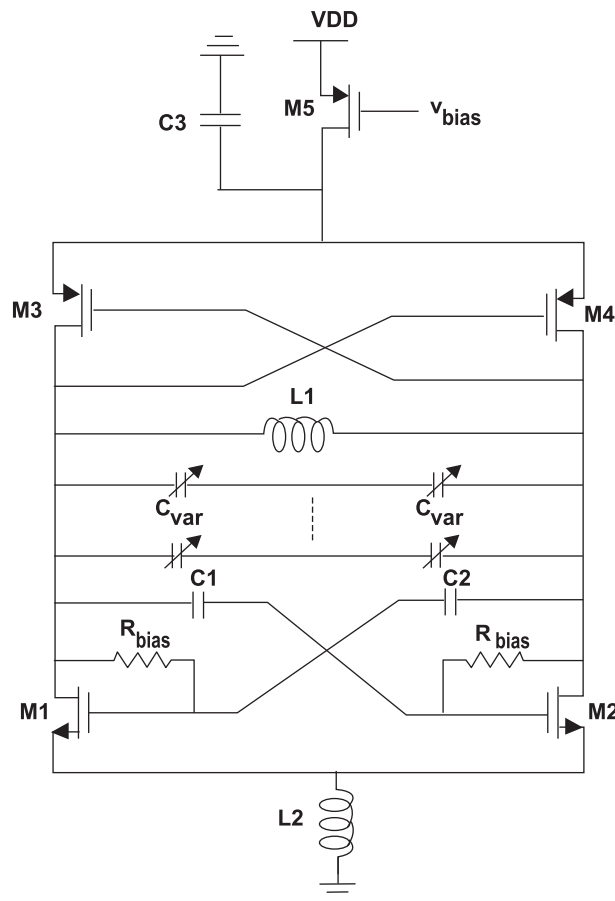


Figure 2. Schematic of proposed LC VCO.

2.1. MOS varactors

A varactor is a voltage-dependent capacitor whose capacitance depends on a control voltage. Due to the main drawback of low maximum to minimum capacitance ratio in deep submicron processes of PN junction varactors, MOS varactors act as tunable elements in the tank circuit. A conventional MOS varactor is designed by source, drain, and bulk terminals connected together, which act as one node of the capacitor, and the other node is the polysilicon gate of the MOS transistor in 0.13 μm CMOS technology. Figure 3a shows the conventional MOS varactor. If control voltage V_{ctrl} varying from -1.5 V to 1.5 V is applied, the corresponding C-V characteristics curve is observed as shown in Figure 3b.

The conventional MOS varactor has three modes of operation: 1) accumulation, 2) depletion, and 3) inversion. The accumulation mode MOS (A-MOS) varactor can be formed by removing the D-S diffusions (p-doped) from the MOS device. The A-MOS varactors and its C-V curve are shown in Figures 4a and 4b. It produces a better quality factor but its tunable region of the C-V curve is very limited.

The inversion mode MOS (I-MOS) varactor is formed by shorting the drain and source terminals to form one capacitor terminal and the gate forms as the other. The bulk terminal of the I-MOS structure is connected to the supply voltage VDD/ground for PMOS/NMOS. To improve the tuning capability further, a large resistance is connected to the bulk and drain terminal of each I-MOS varactor. N-type and P-type I-MOS and modified I-MOS varactors are shown in Figures 5a–5d and its C-V characteristics curves are shown in Figures 6a and 6b.

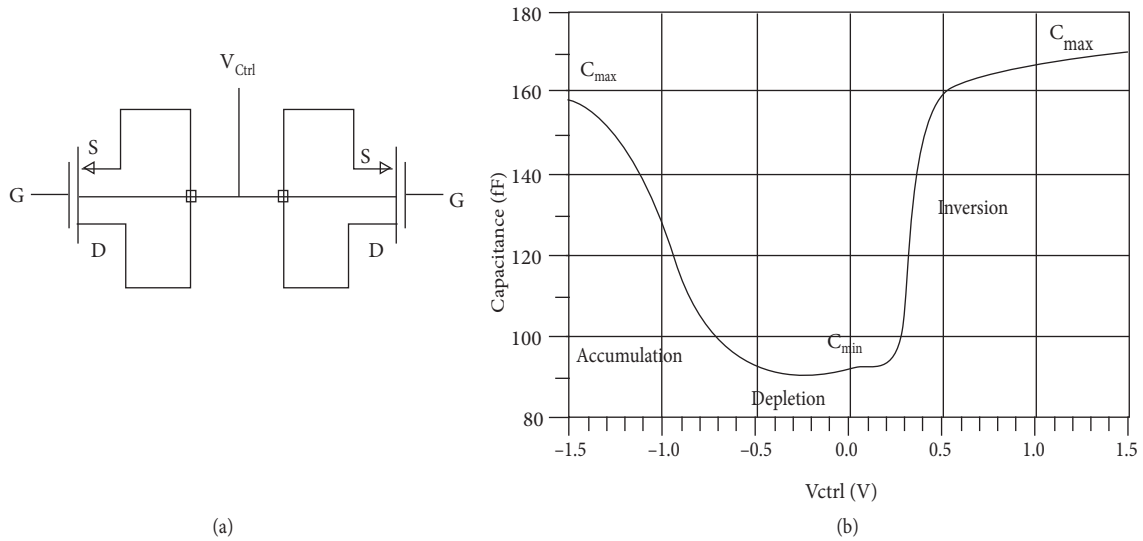


Figure 3. a) Conventional PMOS varactor, b) tuning characteristics.

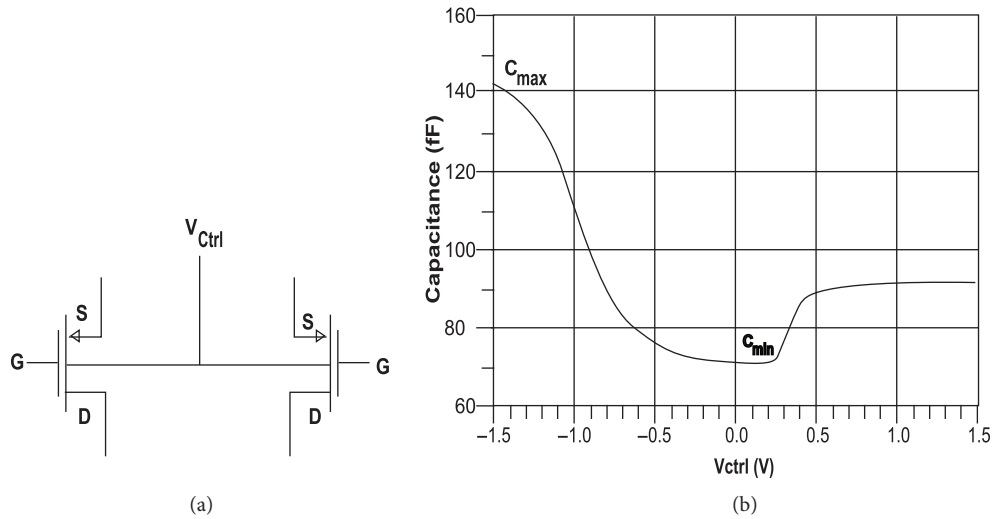


Figure 4. a) AMOS varactor, b) tuning characteristics.

The values of added resistors R_D and R_B are 1500 and 5 k for both PMOS and NMOS. The added resistors are used to reduce the parasitic capacitance, thereby lowering the value of minimum capacitance C_{min} . The tuning range is defined by:

$$TuningRange = \frac{1}{2} \times \frac{C_{max} - C_{min}}{(C_{max} + C_{min})/2} \tag{2}$$

According to the formula, the tuning ranges of the MOS varactors are determined and compared as shown in Table 1. To obtain a wide tuning range, a modified P-type I-MOS varactor with increased tuning range of 48% is preferred for the proposed LC VCO.

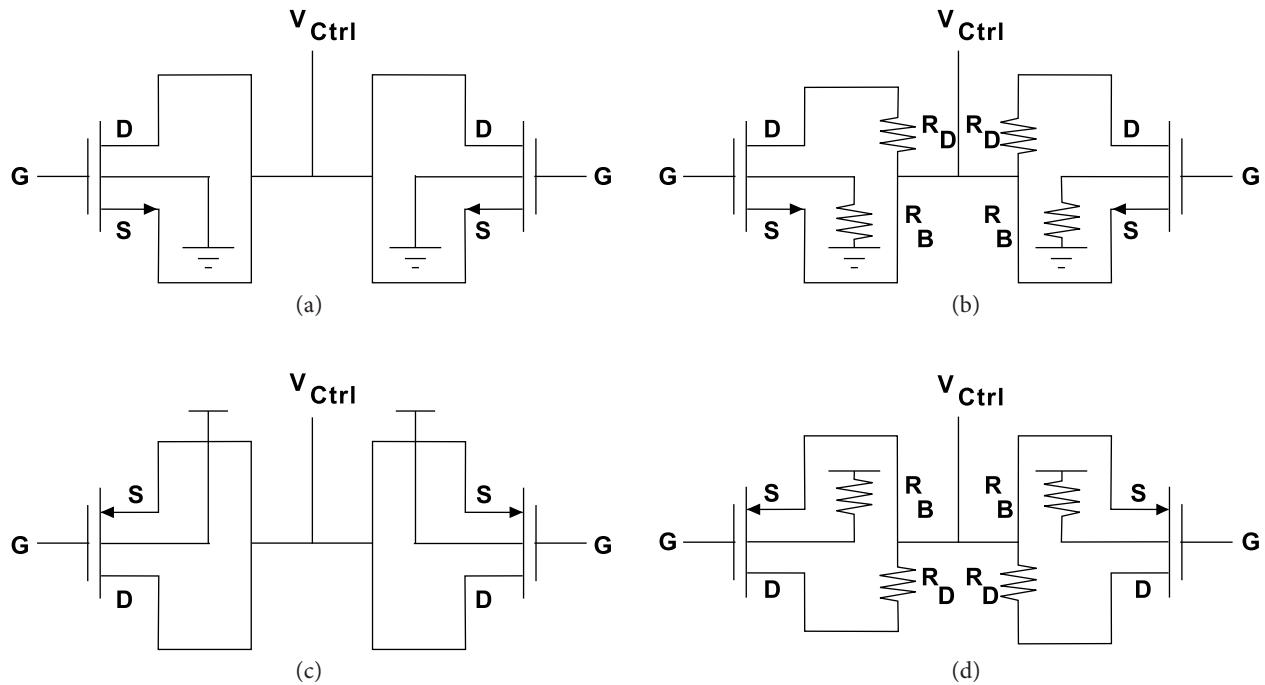


Figure 5. a) I-MOS N-type varactors, b) modified N-type I-MOS varactors, c) I-MOS P-type varactors, d) modified P-type I-MOS varactors.

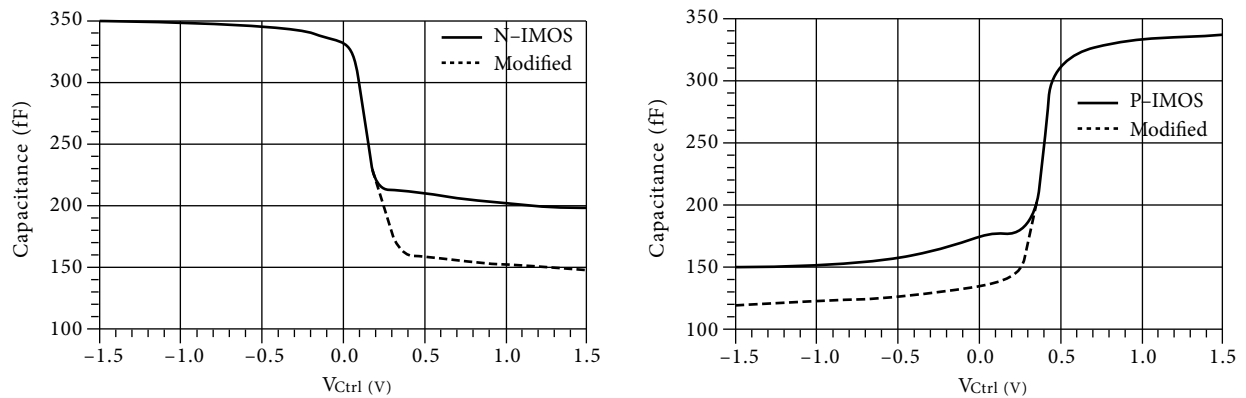


Figure 6. C-V characteristics curve: a) NMOS, b) PMOS varactors.

Table 1. Comparison of MOS varactors.

Type of varactor	Tuning range (%)
A-MOS varactors	33.7
N-type I-MOS varactors	27.5
P-type I-MOS varactors	39
Modified N-type I-MOS varactors	40
Modified P-type I-MOS varactors	48

2.2. On-chip inductor

The LC VCO depends extensively on the performance of high Q integrated inductors. The on-chip inductor is the most important to reduce losses in the LC tank. It depends on most of the design parameters, such as width, shape, thickness, diameter, and spacing, as well as the properties of the material used to implement an inductor. Simple planar spirals are mostly used for RF designs. For any given square spiral, the design variables include width (W), number of turns (N), length or outer diameter (d_{out}), and the interwinding space (S).

A planar spiral inductor is proposed with silicon technology as shown in Figure 7a. The spiral inductor is designed at the 1.2 GHz oscillator’s operating frequency. Figure 7b shows the lumped element model of the on-chip inductor where L and R_s represent the total inductance and resistance of the inductor. Shunt parasitics model the outer winding at Port 1 and the inner winding at Port 2. C_{ox1} and C_{ox2} are the capacitive coupling between the spiral and lossy substrate, C_p is the capacitive coupling between two adjacent spiral tracks, and $R_{si1}, C_{si1}, R_{si2}$, and C_{si2} are substrate parameters.

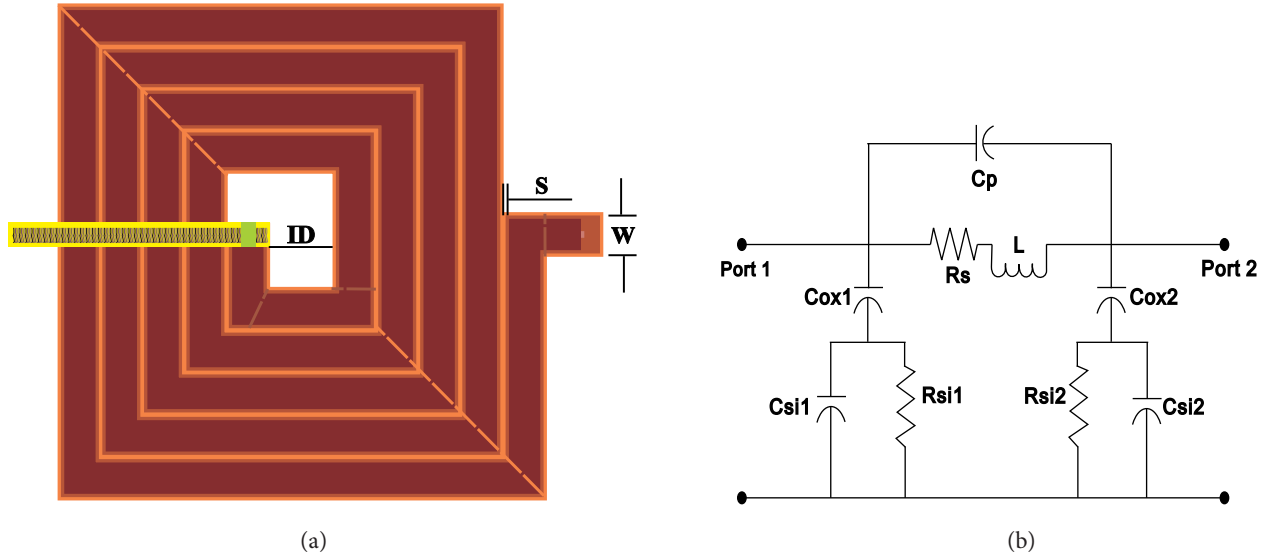


Figure 7. (a) On-chip inductor, (b) pi model.

The design parameters of the spiral inductor are presented in Table 2. Optimum design parameters such as width, spacing, inner dimension, and number of turns have been selected to increase the quality of the inductor.

Table 2. Design parameters of the spiral inductor.

Parameters	Value
Width (μm)	12
Spacing (S) (μm)	1
Inner dimension (ID) (μm)	50
No. of turns	4.5
Electrical length (μm)	1894

The Q factor of the inductor is defined by [12]:

$$Q = 2\pi \frac{\text{Energy stored}}{\text{Energy Loss in one oscillation cycle}} \tag{3}$$

From the Y parameters, the inductance (L) and quality factor (Q) are calculated by [13,14]:

$$L = \frac{imag(1/Y_{11})}{2\pi f} \tag{4}$$

$$Q = -\frac{imag[Y_{11}]}{real[Y_{11}]} \tag{5}$$

where Y11 is the input admittance of the two-port S parameters and f is the frequency in Hz. The simulated inductance value and its Q factor are shown in Figures 8a and 8b. The obtained inductor value is 3.26 nH and its Q factor is 7.7. The optimal selection of design parameters is used to increase the quality factor of 7.7 for inductance value of 3.26 nH.

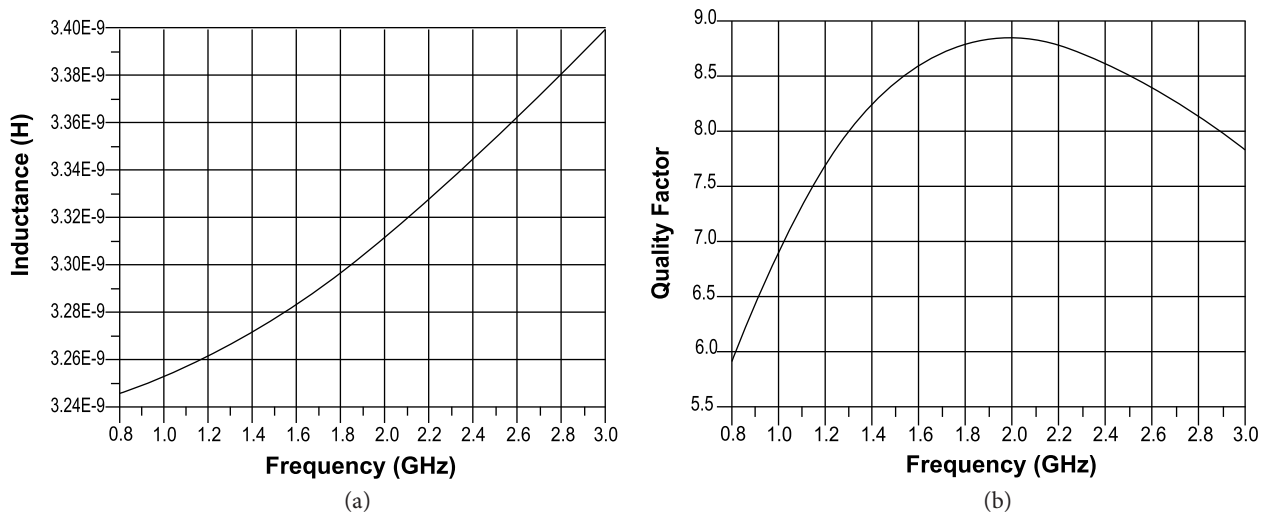


Figure 8. a) Inductance, b) quality factor.

2.3. Phase noise

Phase noise is an important performance measure of the LC VCO. According to Leeson’s model, the phase noise of the oscillator is given by [15]:

$$L(\Delta\omega) = 10\log \left\{ \frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega} \right)^2 \cdot \left(1 + \frac{\Delta\omega_1/f^3}{|\Delta\omega|} \right) \right] \right\} \tag{6}$$

where F is an empirical parameter or unspecified noise factor and k is Boltzmann’s constant. T is the absolute temperature, P_s is the dissipated average power in the resistive part of the tank, ω₀ is the oscillation frequency, Q_L is the effective tank’s quality factor, Δω is the offset from the carrier, and Δω₁/f³ is the corner frequency between the 1/f³ and 1/f² regions. In Eq. (6), the quality factor of the tank is inversely proportional to the phase noise and therefore the quality factor of the tank must be increased to reduce the phase noise. The differential oscillator’s noise factor is specified by [16]:

$$F = 2 + \frac{8\gamma RI_T}{\pi V_0} + \gamma \frac{8}{9} g_{mbias} R \tag{7}$$

where γ is the channel noise coefficient of the MOSFET, I_T is the bias current, and g_{mbias} is the current-source FET's transconductance. From Eq. (7), there are three factors that contribute noise. They are noises due to resistances of the tank, the differential pair of MOSFETs, and the current source. A tank with high quality factor has been designed to reduce noise due to resistances of the tank. The second noise source is produced by thermal noise of FETs. The third component of noise is produced by noise frequencies around the second harmonic [17] and also flicker noise from the tail current source, which enters the LC tank to be up-converted due to the mixing action of the VCO circuit [18]. Usually the tail current transistor is used to set the bias current and also provides the high impedance path to the ground. A large capacitor is added in parallel with the current source, which shunts the noise around the second harmonics to the ground.

In this paper, the current source PMOS transistor is connected at the top of the oscillator since the PMOSFETs have lower flicker noise than the NMOSFETs [19,20]. The top-biased LC VCO restricts substrate noise due to the place of current source in the n-well. The top-biased oscillator allows up-conversion of less flicker noise into phase noise. The tail inductor L2 is inserted at the common source point of the NMOS pair, which is used to reduce the harmonics effect at the output node, lower the voltage headroom, resonate in parallel with the capacitance at that node at $2\omega_0$, and provide high impedance at $2\omega_0$. The inductor value of L2 is 1 nH. The tail PMOS transistor also reduces fluctuations of tail current noise rather than placing the PMOS transistor at the common source point of NMOS transistors [21]. Therefore, the overall phase noise is reduced.

3. Simulation results

The proposed 1.2 GHz LC oscillator has been designed in 130 nm CMOS technology. It is operated under a power supply of 0.8 V. The values of L and C are established on the condition that the angular frequency $\omega_0 = \sqrt{1/LC}$. The tuning curve of the VCO has been obtained by stepping the values of tuning voltage from 0 to 1.5 V as shown in Figure 9. The modified I-MOS varactor tunes the frequency from 1.128 GHz to 1.27 GHz. Using Eq. (2), the tuning range is calculated as 11.7%. Inductance has been designed on the silicon substrate. It has produced the value of 3.26 nH with a quality factor of 7.7.

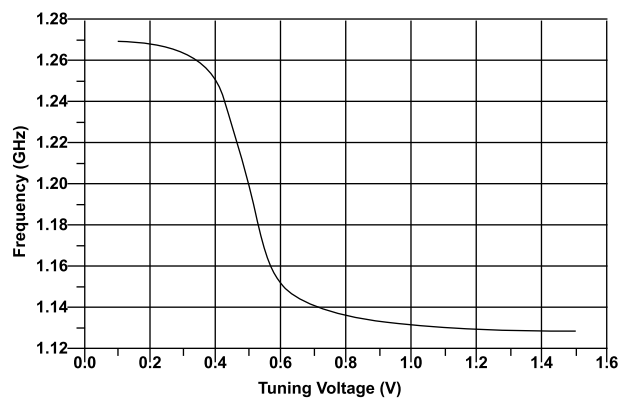


Figure 9. Tuning curve of VCO.

Due to the top-biased coupling inductors, the phase noise is reduced to the value of -132 dBc/Hz as shown in Figure 10. The proposed VCO has drawn 305 μ A current consumption. To compare the performances of the VCO, FOM is calculated by [22]:

$$FOM = L(\Delta\omega) + 10 \log(P_{DC} [mW]) - 20 \log\left(\frac{f_0}{\Delta f}\right) \quad (8)$$

where $L(\Delta\omega)$ represents the phase noise at an offset frequency Δf , P_{DC} is the DC power consumption of the VCO in mW, and f_0 is the oscillation frequency.

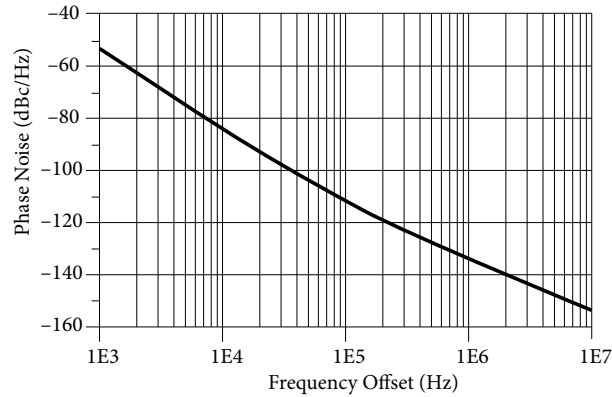


Figure 10. Phase noise of the VCO.

The simulation results of the proposed LC VCO are compared with simulation results of other existing works in Table 3.

Table 3. Comparison of proposed VCO with other existing differential VCOs.

	[7]	[8]	[11]	This work
Technology (nm)	180	65	180	130
Frequency (GHz)	2.4	24.25	3	1.2
Supply voltage (V)	1.2	0.4	0.4	0.8
Power (mW)	1.8	0.94	0.594	0.245
Phase Noise (dBc/Hz)	-131.4 @ 3 MHz offset	-122.5 @ 10 MHz offset	-120.1 @ 1 MHz offset	-132 @ MHz offset
FOM (dBc/Hz)	-187.7	-189.8	-192.1	-199.7

The proposed VCO produces a FOM of -199.7 , which is better than in other works, and the proposed VCO has lower power consumption of 0.245 mW at 800 mV supply voltage. The performances of the proposed VCO are summarized in Table 4.

Table 4. Performance summary of the proposed VCO.

Parameters	Values
Supply voltage	0.8 V
Power consumption	245 μ W
Tuning range	11.7%
Tuning voltage	0–1.5 V
Oscillation frequency	1.2 GHz
Phase noise	-109.3 dBc/Hz @ 100 kHz offset -132 dBc/Hz @ 1 MHz offset

4. Conclusion

A low power low phase noise LC VCO has been designed at a frequency of 1.2 GHz using 0.13 μm CMOS technology. Modified I-MOS varactors and an on-chip inductor with high quality factor have provided a good tuning range. Top biasing with a tail inductor is used to reduce the phase noise. The proposed VCO has produced tuning from 1.128 GHz to 1.27 GHz with a tuning percentage of 11.7%. It has achieved the low phase noise of -132 dBc/Hz at 1 MHz frequency offset and consumed very low power of 245 μW from the voltage supply of 0.8 V.

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