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Investigation of the mechanism of transport across the poly/monocrystalline silicon interface in polysilicon-emitter bipolar transistors based on variations in the interface treatment process

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Abstract: Electrical transport across the poly/monocrystalline silicon (poly-Si/c-Si) interface has been investigated by introducing variations in the interface treatment process affecting the thickness of the native oxide layer formed on the silicon surface. The I-V relationship characterizing the resistance associated with this interface is extracted using an improved open-collector method, which eliminates the inherent nonlinearity arising from the reverse active characteristics of the bipolar transistor. The nonohmic behavior of the interface at low electric fields is demonstrated to be consistent with direct tunneling through a rectangular barrier presented by an ultrathin interfacial oxide layer. An approximate tunnel junction model is proposed that fits the tunneling current in the low bias regime, predicting the experimentally observed increase in the low-voltage leakage current associated with ultrathin oxides. The thickness of the interfacial oxide extracted by fitting the measured data to the proposed rectangular-barrier tunnel junction model is in good agreement with reported experimental values. Finally, a relation between experimentally introduced variations in the interface treatment process and the magnitude of the resistance associated with the interface is identified, which can be quantitatively explained based on the direct tunnel junction model in terms of differences in the native oxide thickness.

Key words: Heterojunction bipolar transistor, polysilicon emitter, semiconductor-insulator interfaces, series emitter resistance, tunneling

1. Introduction

Given the unceasing drive toward scaling and enhancement of the high-frequency performance of bipolar integrated circuit technologies, characterization and modeling of advanced bipolar transistors continue to generate considerable research interest [1–4]. In particular, measurement and extraction of the emitter series resistance, r_E, in silicon/germanium (SiGe) heterojunction bipolar transistor (HBT) device technology has been the topic of recent investigations [5–7]. Accurate measurement of r_E for model parameter extraction is of critical importance for proper design of high-speed bipolar analog integrated circuits. As the emitter area is reduced the emitter resistance increases inversely with the emitter area to the first approximation, causing a severe degradation in the device transconductance. In addition, the voltage drop across the emitter series resistance at high currents has a significant influence on the DC bias and contributes to device mismatch. The poly/monocrystalline silicon (Poly-Si/c-Si) interface present at the emitter of polysilicon-emitter bipolar transistors has also attracted significant recent interest as a passivating contact enhancing silicon solar cells conversion efficiency [8–10]. As compared with traditional bipolar transistors employing metal-contacted emit-

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ters, in advanced bipolar transistors using polysilicon emitters such as SiGe HBTs an increase in the current gain, β, resulting from a corresponding decrease in the back-injected component of the base current is obtained at the expense of a rise in the emitter series resistance gain [11, 12]. Specifically, in SiGe HBTs r_E comprises the polysilicon sheet resistance, the resistance associated with the poly/monocrystalline silicon (Si) interface, the resistance of the silicide-polysilicon interface, and the resistance of the standard ohmic metal-semiconductor contact [7]. Considering the typical contribution of the different components of r_E to the overall resistance, the observed increase in the emitter series resistance is generally ascribed to the poly/monocrystalline Si interface, where an ultrathin oxide layer is formed between the emitter polysilicon and the base region prior to deposition of polysilicon [12]. Furthermore, r_E exhibits a grossly nonohmic behavior at low emitter currents, which is presumed to be associated with the mechanism of carrier transport across the emitter interface. In fact, based on theoretical calculations, the back-injected component of the base current has been argued to result from tunneling of holes through the interfacial oxide [13].

Although tunneling through the interfacial oxide has been studied theoretically [13, 14], it has not been demonstrated based on actual measurements of the current flow through the emitter terminal. According to the only empirical investigation focusing on direct tunneling across the polysilicon emitter interface, a rectangular-barrier model for tunneling can be justified indirectly based on the $I_B - V_{BE}$ characteristics of the device given the proportionality of the tunneling current flowing through the emitter terminal to the base current [15]. Estimation of the tunneling current using the base current, however, requires that the bias dependence of the base resistance as well as current gain roll-off at low collector currents be taken into account. One of the main challenges in experimental verification of a proposed mechanism for transport across the emitter interface is to distinguish between the nonlinearity characteristic of the specific mechanism and the nonlinearities inherent to the DC operation of the bipolar transistor. The inherent nonlinearities, which commonly influence the measurement results obtained using the popular open-collector method for characterization of r_E, are due to the Kirk effect and the substrate bias [16, 17]. In this work, the nonlinear I-V characteristics associated with transport across the polysilicon emitter interface are extracted based on correction of the standard open-collector method. The nonohmic behavior of the interfacial resistance is evaluated to determine whether direct tunneling is the dominant transport mechanism. An approximate model for direct tunneling is proposed to achieve an accurate fit to the measured tunneling current traversing ultrathin oxides in the low bias regime, where an increased leakage current is commonly observed. In addition, existence of a relation between experimental variations in the interface treatment process and the value of the interfacial resistance is investigated based on the rectangular tunnel junction model.

2. Materials and methods

In this section relevant experimental details of the device fabrication process employed are presented. In addition, the experimental setup for the measurement of the emitter series resistance under open-collector conditions using the semiconductor parameter analyzer is specified. In order to study the mechanism of transport across the polysilicon/monocrystalline Silicon interface, the nonlinear device characteristics impacting the measurement of the interfacial resistance have to be corrected. To this end, an improved-open collector method is introduced for measurement of r_E, which allows isolation of the nonlinear characteristics arising specifically from the nonohmic behavior of the interfacial resistance. Finally, the dependence of the emitter series resistance on the thickness of the interfacial oxide is evaluated based on experimental variations in the interface treatment process known to affect the native oxide thickness.

2.1. Device fabrication

The bipolar transistors used for the study of transport at the poly-Si/c-Si interface were fabricated in a 0.8 μm BiCMOS process employing standard LOCOS techniques. A lightly doped 10 Ωcm p-type (100) oriented wafer was employed as the substrate material in which the $n+$ buried layer regions were formed by using an antimony implant followed by a diffusion step. A thin $(1.1 - 1.5\ \mu\text{m})$ arsenic-doped epitaxial layer with an approximate resistivity of 1 Ωcm formed the collector region. The base regions were patterned and ion-implanted using boron. Arsenic-doped LPCVD polysilicon was employed to form the emitter contact. The final doping profile was characterized by approximate junction depths of 0.1 μm and 0.2 μm for the base-emitter and base-collector junctions, respectively, with the doping concentrations of the collector, base, and emitter approximately equal to 5×10^{15} cm^{-3}, 4×10^{17} cm^{-3}, and 10^{20} cm^{-3}, respectively. The mask dimensions of the emitter width and length were 3 μm and 1.2 μm, respectively.

2.2. Device characterization

Measurements of the emitter series resistance were carried out under open-collector conditions using the HP4145A semiconductor parameter analyzer. Specifically, with the emitter grounded the external base current, which flows across the base-emitter junction into the emitter under OC conditions, was swept using a stimulus/monitoring unit (SMU). Another SMU was used to force the collector current to zero simultaneously, allowing measurement of the floating collector voltage. The resolution of the HP4145A over the range of the measured collector voltages is 1 mV. For more sensitive voltage measurements the HP4156 was used, the 2 μV resolution of which is roughly three orders of magnitude higher. Measurements were performed under dark conditions.

2.3. The improved open-collector method

The standard open-collector method is a common and widely studied measurement method for direct extraction of the emitter series resistance [17, 18]. In this method, with the collector left floating, the externally applied base current, I_B, flows across the base-emitter junction into the emitter terminal, and $I_E = I_B$. With $I_C = 0$ the transistor is driven to operate in the saturation region. Using the Ebers–Moll model the measured collector-emitter voltage for an npn transistor operating in the saturation region, i.e. V_{CES}, can be expressed as

$$V_{CES} = -(\frac{kT}{q})ln\alpha_I + r_E I_E, \tag{1}$$

where α_I represents the common-base current gain in the reverse active mode, which is given by the ratio of the emitter to the collector current; I_E is the emitter current corresponding to the externally applied base current; and finally T, k, and q denote the absolute temperature, the Boltzmann constant, and the charge of an electron, respectively. The value of the emitter resistance r_E is obtained by measuring V_{CES} as a function of the applied base current. If the common-base current gain, α_I, is assumed to be independent of the emitter current, from Eq. (1), the value of r_E will be given by the slope of the $V_{CES} - I_E$ plot.

While the open-collector (OC) method is a convenient DC characterization method, the nonlinearities commonly present in the $V_{CES} - I_E$ characteristics render the extraction of a bias-independent value for r_E represented by $\frac{\partial V_{CES}}{\partial I_E}$ complicated, causing ambiguity in interpretation of the measurement results. The nonlinearities arise from the characteristics of the transistor in the reverse active mode, as well as the nonlinearity ascribed to high-injection effects including conductivity modulation due to the Kirk effect [16, 17]. The emitter

series resistance is generally considered to be the slope of the $V_{CES} - I_E$ plot corresponding to higher emitter currents, for which high injection effects are relevant. Therefore the nonlinearity observed in the high-current region has been attributed to the lack of inclusion of the high-injection effects in the Ebers–Moll model [16, 17] describing the OC characteristics given by Eq. (1). However, in the low-current region, where the nonlinearity is speculated to result from transport across the emitter contact, high injection effects are inconsequential. The nonlinearity originating from the high injection effects can be considered as an inherent source of nonlinearity, which is independent of the specific structure of the emitter contact. Another source of inherent nonlinearity emanating from the reverse characteristics of the transistor is the variations in the reverse current gain α_I with the emitter current given by the first term in equation Eq. (1). An estimation technique involving postprocessing of the measured data has been developed based on measurement of the reverse characteristics of the transistor to improve the accuracy of the OC method. In particular, by characterizing α_I as a function of the emitter current, a corrected open-collector voltage $V_{CES_{cor}}$ can be calculated from $V_{CES_{cor}} = V_{CES} + (\frac{kT}{q})ln(\alpha_I) = r_{E_{cor}} I_E$. The slope of the $V_{CES_{cor}} - I_E$ plot, $r_{E_{cor}}$, specifies the corrected value of the emitter series resistance.

2.4. Variation of the interface treatment process

In order to assess the dependence of the emitter series resistance on the interfacial oxide, the improved open-collector method was applied to measure r_E in devices belonging to a split lot of wafers fabricated in the given BiCMOS technology receiving two different interface treatments. The oxidizing RCA-1 cleansing treatment followed by a brief 5-s etch in 50:1 DI:HF (deionized water to HF ratio) was performed prior to polysilicon deposition on a number of wafers, while the remaining wafers in the split lot only received a 15-s etch in 50:1 DI:HF etch prior to polysilicon deposition so as to remove any interfacial oxide.

3. Experimental results

The nonohmic behavior of the emitter contact at low emitter currents was characterized based on the proposed corrective scheme in order to evaluate direct tunneling as the mechanism of transport across the interface. In addition, dependence of the emitter series resistance on variations in the interface treatment process, which influence the native oxide thickness was evaluated.

The improved OC method was employed to characterize the interfacial component of the emitter series resistance in *npn* implanted-base Si bipolar junction transistors (BJTs) with polysilicon emitters fabricated in the given submicron BiCMOS process. It is noteworthy that the trade-off between a high value of current gain and a large value of emitter resistance observed with regard to the devices characterized in this work also applies to the operation of more advanced devices employing epitaxial bases. This is due to the fact that implanted-base Si bipolar junction transistors and epitaxial-base HBTs basically share an identical structure for the emitter contact. Specifically, regardless of whether the base material is SiGe or plain Si, an advanced *npn* silicon-based bipolar transistor employs a relatively thick arsenic-doped $n+$ polysilicon film in the emitter [11, 19]. The typical measured $V_{CES} - I_E$ characteristics obtained using the standard OC method and a plot of the slope of these characteristics representing r_E are shown in Figure 1 and Figure 2 respectively. Evidently, the emitter series resistance is characterized by grossly nonohmic behavior at low emitter currents, which may be attributed to the interfacial resistance. At higher bias currents, the nonlinearity is less severe as confirmed by the relatively ohmic behavior of the $V_{CES} - I_E$ characteristics, represented by the reletively constant value of the slope. As pointed out, the slope of the characteristics in the high-bias regime is commonly adopted as the value of r_E. The correction scheme was applied to the measured $V_{CES} - I_E$ characteristics obtained using the standard

open-collector method. In particular, the nonlinear term in Eq. (1) was eliminated based on measurement of α_I, whose typical dependence on emitter current is shown in Figure 3, allowing determination of the corrected open-collector voltage $V_{CES_{cor}}$ as a function of I_E. The slope of the $V_{CES_{cor}} - I_E$ thus obtained represents the corrected value of the emitter series resistance, which is compared with that obtained using the standard open-collector method in Figure 4. As indicated, applying the improved OC method to characterize r_E leads to improvements in accuracy on the order of 10 percent.

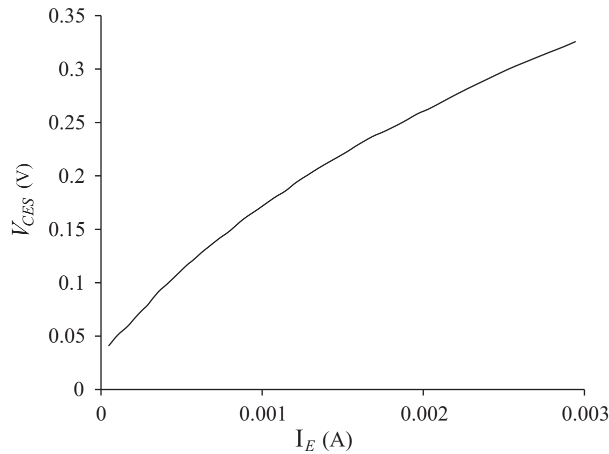

Figure 1. Collector-emitter saturation voltage, V_{CES}, versus emitter current, I_E, measured using the standard open-collector method with floating substrate.

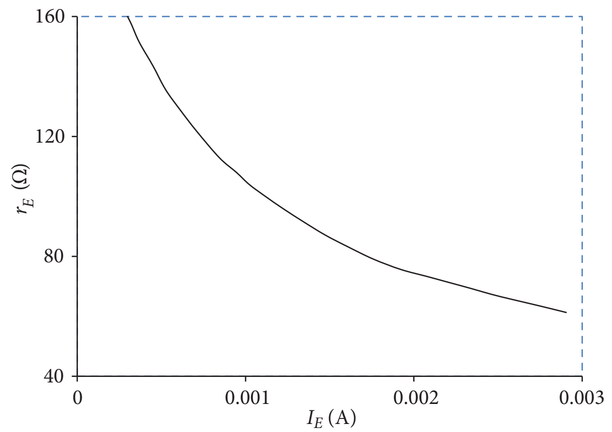

Figure 2. Series emitter resistance, r_E, versus emitter current, I_E, measured using the standard open-collector method with floating substrate, $A_E = 3\ \mu m \times 1.2\ \mu m$.

The dependence of the emitter series resistance on the thickness of the interfacial oxide was also evaluated based on experimental variations in the interface treatment process. Notably, application of an oxidizing cleansing treatment, such as the RCA cleansing procedure, prior to polysilicon deposition is known to lead to formation of a thin oxide layer, while a nonoxidizing precleaning treatment followed by a hydrogen fluoride (HF) etch can be employed to remove the interfacial oxide. The variations of r_E with I_E determined based on the improved OC method for a device whose processing involved the RCA procedure as well as those for a transistor undergoing only the HF etch prior to polysilicon deposition are shown in Figure 5. As is evident, at a given emitter current the measured value of the emitter series resistance corresponding to the RCA cleansing procedure was significantly higher than that for devices undergoing only the HF etch in the low emitter current range, indicating that a smaller value of r_E is obtained as the interfacial oxide thickness is reduced. Using the more sensitive HP4156 semiconductor parameter analyzer the value of the emitter series resistance at $V_{CES_{cor}} = 40$ mV corresponding to the RCA cleansing procedure was determined to be approximately 275 Ω based on the improved OC method, while that associated with the HF etch at the same value of $V_{CES_{cor}}$ was approximately 40 Ω, indicating that a smaller value of r_E is obtained as the interfacial oxide thickness is reduced. Furthermore, Figure 5 indicates that the emitter resistance in RCA transistors exhibits a more significant nonlinearity at low emitter currents.

4. Theoretical analysis

In this section an approximate model for transport across the emitter interface is developed to fit the experimental data obtained using the improved OC method.

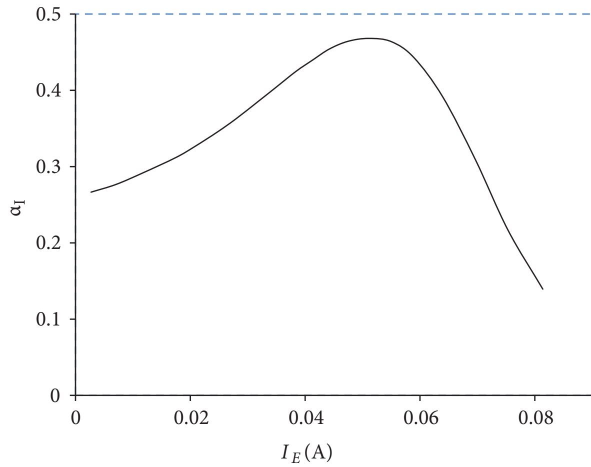

Figure 3. Typical variation of the common-base current gain in the reverse active mode, with the emitter current $A_E = 3\ \ \mu m \times 1.2\ \ \mu m$.

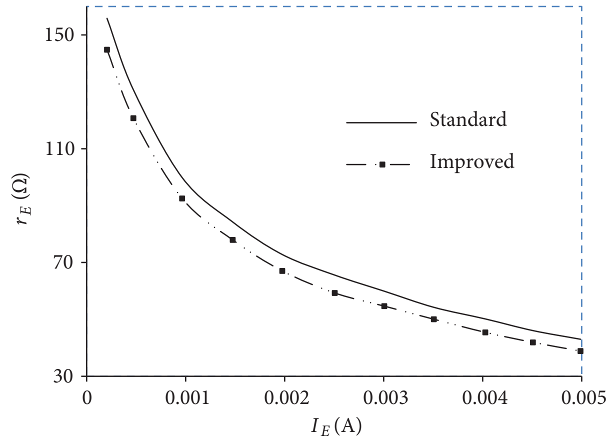

Figure 4. Measured versus corrected emitter series resistance as a function of emitter current, I_E, based on the open-collector method.

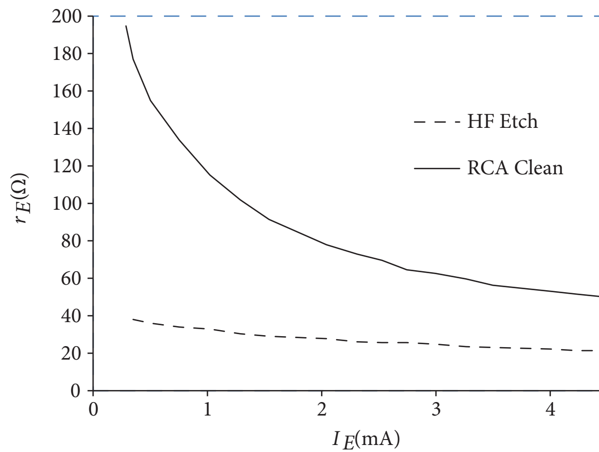

Figure 5. Measured emitter series resistance as a function of emitter current, I_E, based on the improved open-collector method for two different surface treatment processes.

4.1. Modeling of transport at the poly/monocrystalline silicon interface

The nonohmic behavior of the emitter series resistance has been theoretically evaluated based on a tunnel junction model by assuming the presence of a rectangular potential barrier at the emitter interface [13]. This model, however, has not been verified empirically, presumably since measurement of the interfacial resistance from the terminal characteristics of the transistor has turned out to be a difficult undertaking.

A model for direct tunneling across the Si/SiO_2 interface proposed for MOSFETs has been employed [20] to determine whether tunneling through a rectangular barrier occurs across the emitter interface. This model was proposed as an enhancement to a widely employed model for direct tunneling across the MOSFET gate oxide [20] to allow for the tunneling current to approach zero as the oxide voltage tends to zero. According to

this model, for a rectangular barrier the tunneling current density, J_{te}, is given by [20]:

$$J_{te} = AE_{ox}^2 exp\left\{-\frac{B\left[1-(1-\frac{qV_{ox}}{\phi_b})^{\frac{3}{2}}\right]}{E_{ox}}\right\}, \tag{2}$$

where E_{ox} is the electric field across the oxide given by $\frac{V_{ox}}{t_{ox}}$ with V_{ox} and t_{ox} representing the oxide voltage and the thickness of the oxide, respectively, and the preexponent A with units of A/V^2 and the parameter B with units of V/m are given by the following expressions:

$$A = \frac{q^3 m_e}{8\pi h m_{ox}\phi_b}, \tag{3}$$

$$B = \frac{8\pi(2m_{ox})^{1/2}{\phi_b}^{3/2}}{3hq}, \tag{4}$$

where m_e and m_{ox} denote the free electron mass and the carrier effective mass in the oxide, respectively; h is Plank's constant; and ϕ_b represents the barrier height for the electron associated with electron tunneling from the conduction band. According to Schuegraf's model given by Eq. (2), absent the dependence of the exponential term on E_{ox}, a linear relationship exists between $\sqrt{J_{te}}$ and V_{ox}. This is in fact the case in the low bias regime where the exponential term in Eq. (2) becomes approximately constant in the $qV_{ox} << \phi_b$ range. Specifically approximating $(1-q\frac{V_{ox}}{\phi_b})^{3/2}$ as $(1-\frac{3qV_{ox}}{2\phi_b})$ in the low-bias regime, the exponential term in Eq. (2) is simplified to the field-independent term $exp\left(-\frac{3qBt_{ox}}{2\phi_b}\right)$. Following the introduction of an experimental fitting parameter n, Eq. (2) yields an expression for the tunneling current density as follows:

$$J_{te} = AE_{ox}^2 exp\left(-\frac{3qBt_{ox}}{2n\phi_b}\right). \tag{5}$$

The parameter n is an ideality factor with a nominal value of unity, which can be adjusted to obtain an accurate fit to the measured gate current characteristics. In practice, the value of n can be extracted from the experimental data based on an independent measurement of oxide thickness, e.g., using ellipsometry.

Presence of a rectangular barrier at the emitter interface is confirmed by fitting the I-V characteristics of the interfacial resistance obtained using the improved OC method to the approximate tunnel junction model given by Eq. (5) derived from Schuegraf's direct tunneling model. Noting that $V_{CES_{cor}}$ is equivalent to the potential drop across the emitter resistance, the existence of a tunneling current flowing through the emitter terminal can be determined by examining whether a linear relation between the square root of the emitter current density, $\sqrt{J_E}$, and $V_{CES_{cor}}$ holds. Applying the proposed corrective scheme to typical $V_{CES} - I_E$ characteristics obtained using the standard OC method, in fact, indicates that $\sqrt{J_E}$ exhibits a strong linear correlation with $V_{CES_{cor}}$ in the 40 mV $< V_{CES_{cor}} <$ 130 mV range as demonstrated in Figure 6. The modeled-versus-measured fit of Figure 6 was obtained using the typical values $m_{ox} = 0.40m_e$ with the free electron mass $m_e = 9.1\times10^{-31}$ kg, and $\phi_b = 3.1$ eV and $n = 1.218$. The value of the oxide thickness can be estimated based on the extension to Schuegraf's model using the $\sqrt{J_E} - V_{CES_{cor}}$ data of Figure 6. To this end, the expression for the slope of the $\sqrt{J_{te}}$ versus V_{ox} curve is derived as $\left(\frac{\sqrt{A}}{t_{ox}}\right) exp\left(-\frac{3qBt_{ox}}{2n\phi_b}\right)$ from the proposed model given

by equation Eq. (5). Based on this expression for the slope, t_{ox} is extracted to be approximately 4.9 Å given the experimental value of the slope indicated in Figure 6.

The approximate model proposed as an extension to Schuegraf's model fits the measured gate current versus gate bias characteristics in the sub-0.5 V range in MOSFETs featuring gate oxide thicknesses in the range of a few tens of nanometers. Specifically, data presented in support of a semiempirical model for gate tunneling currents [21] has been fitted to the approximate model given by Eq. (5) producing the linear, modeled-versus-measured $\sqrt{J_g} - V_{ox}$ characteristics of Figure 7 using $m_{ox} = 0.40m_e$, $\phi_b = 3.1$ eV, and $n = 1.25$. Based on the expression for the slope of the $\sqrt{J_{te}}$ versus V_{ox} curve derived from Eq. (5), namely $\left(\frac{\sqrt{A}}{t_{ox}}\right) exp\left(-\frac{3qBt_{ox}}{2n\phi_b}\right)$, the oxide thickness is extracted to be 24.8 Å using the experimental characteristics slope given in Figure 7. The extracted value matches that obtained based on the semiempirical model of Lee et al. [21] exactly.

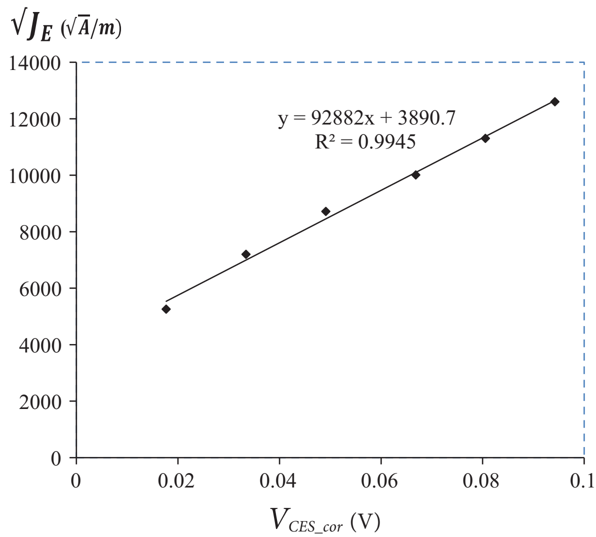

Figure 6. $\sqrt{J_E} - V_{CES_{cor}}$ obtained using the improved open-collector method $A_E = 3\ \ \mu m \times 1.2\ \ \mu m$.

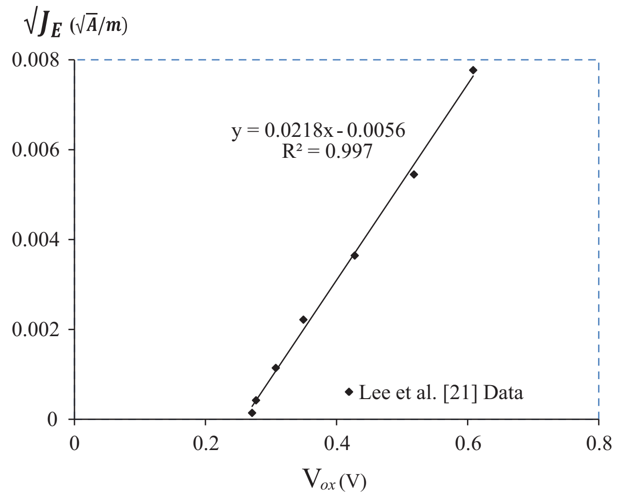

Figure 7. Modeled-versus-measured $\sqrt{J_g} - V_{ox}$ obtained using the proposed extension of Schuegraf's model for electron tunneling from the conduction band based on data reported by Lee et al. [20].

4.2. Modeling of the interfacial emitter resistance

Given the empirical evidence supporting a rectangular-barrier tunnel junction model for the emitter contact, Eq. (2) can be employed to readily obtain an approximate expression for the interfacial component of the emitter resistance. Expressly, since the interfacial resistance is associated with the low-bias regime, we may apply the approximation $(1 - q\frac{V_{ox}}{\phi_b})^{3/2} \approx 1$ for $qV_{ox} << \phi_b$, based on which Eq. (2) gives the expression for the electron tunneling current as follows:

$$I_{te} = A_{tj} A {E_{ox}}^2 = \left(\frac{A_{tj} A}{{t_{ox}}^2}\right) {V_{ox}}^2, \tag{6}$$

where A_{tj} represents the area of the tunnel junction. Therefore, using Eq. (6), the interfacial component of the emitter resistance, $r_{E_{Intrfc}}$, defined as $r_{E_{Intrfc}} = \frac{1}{\frac{\partial I_E}{\partial V_{CES_{cor}}}}$ for a given operating point $\left(V_{CES_{0_{cor}}}, I_{E_0}\right)$, can be

written as:

$$r_{E_{Intrfc}} = \left(\frac{{t_{ox}}^2}{2A_E A V_{CES_{cor}}} \right), \tag{7}$$

where A_E denotes the emitter area and is equivalent to A_{tj}. Thus, the experimental results on the variation of the emitter series resistance with the interface treatment process may be evaluated quantitatively in terms of the simple expression for $r_{E_{Intrfc}}$ given by Eq. (7). In particular, considering the reciprocal of the ratio of the measured emitter series resistance associated with the RCA cleansing treatment to that resulting from the HF etch treatment at $V_{CES_{cor}} = 40$ mV, namely $40/275 = 0.145$, from Eq. (7) we expect the thickness of the interfacial oxide for devices receiving the HF etch to be $\sqrt{0.145} = 0.38$ times that for the transistors subject to the RCA procedure. Therefore, assuming that the $tox = 4.9$ Å value extracted from the $J_E - V_{CES_{cor}}$ data for devices having received the RCA treatment is valid, the thickness of the interfacial oxide for devices subject to the HF etch is expected to be about 1.9 Å. This value is close to the typical accuracy of the ellipsometry technique, implying that the 15-s HF etch has substantially removed the native oxide. This implication is confirmed by the relatively small variation in the emitter resistance in the device having received the longer HF etch as indicated in Figure 5. However, the nonlinear behavior still persists at lower emitter currents, indicating that the oxide has not been completely removed.

5. Discussion

An elaborate interpretation of the OC measurement results was proposed by Gabl et al. [17] based on a detailed model for the measurement-induced nonlinearity under conditions of high-level injection at the collector and the base. Given the absence of high injection effects in the low-field bias range relevant to characterization of tunneling, the simple approach employed herein to correct the OC method proved adequate for identification of the transport mechanism at the emitter interface. Specifically, this approach allowed characterization of the electron tunneling current traversing the native oxide present at the poly/monocrystalline silicon interface in the absence of electrical contact to the active emitter region. A reasonable value of 4.9 Å extracted for the interfacial oxide thickness from the experimental data based on the extension to the direct tunneling model of Schuegraf et al. [20] was obtained without adopting the effective mass and barrier height as fitting parameters. This value is also in agreement with the typical value of 6.7 Å reported for the thickness of the native oxide formed on the surface of a bare silicon wafer exposed to room-temperature air in a clean room over a period of 7 days [22]. For the devices characterized in this work, which had received RCA treatment prior to polysilicon deposition, the extracted value of oxide thickness was lower than the typical value of 20 Å reported for the oxide thickness at heat-treated, poly/monocrystalline interfaces [23]. The latter observation may be partially explained by the 5-s HF dip performed following the RCA-1 procedure. Nevertheless, the extracted value may not be accepted as the thickness of the native oxide at the polysilicon emitter interface without independent confirmation, e.g., based on the ellipsometry technique.

Schuegraf's model has been noted to overestimate the tunneling current in the low bias regime, failing to provide an accurate fit to the experimental data in the sub-1-V gate bias range, where a significant oxide leakage current is observed [21]. Accordingly, Lee et al. [21] proposed an elaborate semiempirical model incorporating a correction function, which accounts for the empirical data over the whole bias range and permits accurate extraction of the oxide thickness. On the other hand, the results presented herein indicate that if the goal is to obtain an accurate characterization of the leakage current in the low-bias regime, the approximate model

proposed as a simple extension of Schuegraf's model is adequate. Specifically, with the introduction of an experimental fitting parameter, n, equivalent to an ideality factor, the proposed extension accurately fits the measured gate current data of Lee et al. [21], allowing extraction of an oxide thickness value, which is in good agreement with that reported based on ellipsometry. In practice, the fitting parameter, n, enables attainment of a reasonable match to experimental data by fitting the effective mass and the barrier height within a narrow range so as to compensate for the inaccuracy resulting from the WKB approximation.

In another empirical investigation on tunneling across the polysilicon emitter interface Ricco et al. [15] likewise identified direct tunneling through an ultrathin interfacial oxide as the dominant transport mechanism. Specifically, assuming a constant tunneling probability it was established that the tunneling current density varies with the square of the electric field across the oxide in the low-bias regime [15]. Considering the polysilicon-insulator-silicon interface as a metal-oxide-semiconductor (MOS) capacitor biased in the accumulation region Ricco et al. et al. [15] gave the expression for the electron tunneling current density, J_{te}, as $qv_{th}P_e\frac{{\epsilon_{ox}}^2}{2kT\epsilon_{Si}t_{ox}^2}V_{ox}^2$, where v_{th} represents the thermal velocity of the electron, ϵ_{Si} and ϵ_{ox} designate the dielectric constant of Si and the oxide, respectively, and P_e is the electron tunneling probability. Given a constant barrier height for the electron, using the WKB approximation, the electron tunneling probability can be expressed as $exp\Big[-\Big(\frac{2\sqrt{2m_{ox}\phi_b}}{\hbar}\Big)t_{ox}\Big]$ with $\hbar$ denoting the reduced Plank's constant. The expression for the slope of the $\sqrt{J_{te}}$ versus V_{ox} curve based on Ricco's model is given by $\sqrt{\frac{qA_{tj}v_{th}P_e}{2kT\epsilon_{Si}}}(\frac{\epsilon_{ox}}{t_{ox}})$; using the latter expression, the oxide thickness is extracted from the slope of the $\sqrt{J_E} - V_{CES_{cor}}$ plot of Figure 6 to be roughly 7.3 Å with $v_{th} = 10^5$ m/s, $m_{ox} = 0.40m_e$, and $\phi_b = 3.1$ eV. The value of t_{ox} extracted from the experimental data presented in this work using Ricco's model is in excellent agreement with the 7 Å value reported by Ricco et al. [15] based on an indirect approach requiring simultaneous characterization of the current gain of the transistor. The approximately 7 Å value for oxide thickness predicted by Ricco's model is also in excellent agreement with the typical value of 6.7 Å reported for the native oxide [22].

Moreover, Fowler–Nordheim (FN) tunneling through a triangular potential barrier can be ruled out as the dominant transport mechanism at the polysilicon-emitter interface. Specifically, considering the expression for the FN tunneling current density [24, 25] given by $J_{t_{FN}} = A{E_{ox}}^2exp\Big(-\frac{B}{E_{ox}}\Big)$, absence of the FN tunneling mechanism at the polysilicon-emitter interface has been verified by evaluating $\ln\Big(\frac{J_E}{E_{ox}^2}\Big)$ as a function $\frac{1}{E_{ox}}$ using typical $V_{CES_{cor}} - I_E$ characteristics and noting the lack of existence of a strong linear correlation between these quantities [26]. The lack of dominance of FN tunneling at the emitter contact is consistent with the observation that FN tunneling dominates for thicker oxides and is independent of thickness, whereas direct tunneling occurs in thinner oxides at low fields [27]. Generally, direct tunneling is limited to oxides thinner than 50 Å, implying that experimental constraints, such as current sensitivity of characterization tools and the effective device area, limit observation of direct tunneling currents [20]. Presence of a triangular-shaped potential barrier, attributed to dopant pile-up at the polysilicon emitter interface, has been inferred for those interfacial layers having received RCA cleansing surface treatment [28]. Our analytical and experimental results, however, do not support this assertion.

The observed variation in the magnitude of the emitter resistance in response to two different interface treatments, namely the RCA-1 procedure and the etch in HF, can be explained in terms of the influence

of the given treatment on the thickness of the interfacial oxide. Specifically, according to the expression for the interfacial component of the emitter resistance derived using the approximate rectangular-barrier tunnel junction model, this component varies in proportion to the square of the oxide thickness. The ratio of the oxide thicknesses corresponding to each treatment estimated as the square root of the ratio of the corresponding values of the measured interfacial resistance indicated that the native oxide thickness for devices receiving the HF etch was reasonably smaller than that for devices undergoing the RCA procedure.

Conclusion

A correction to the OC method allowed extraction of the I-V characteristics of the nonlinear interfacial resistance present at the polysilicon emitter contact, which was shown to fit an approximate tunnel junction model corresponding to a rectangular potential barrier. The extracted value of the oxide thickness is in agreement with that of the native oxide that forms on the surface of silicon at room temperature. An approximate model for the tunneling current through thin interfacial oxides was proposed that fits the experimental gate current data in the low-bias regime, allowing accurate extraction of the oxide thickness. Finally, a simple rectangular-barrier tunnel junction model for the emitter contact was demonstrated to quantitatively explain the influence of the variations in the interface treatment process on the magnitude of the interfacial resistance in terms of differences in oxide thickness.

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References

[1] Voinigescu S, Dacquay E, Adinolfi V, Sarkas I, Balteanu A et al. Characterization and moldeling of an SiGe HBT technology for transceiver applications in the 100–300-GHz range. IEEE Transactions on Microwave Theory and Techniques 2012; 60: 4024-4034.

[2] Zekry A, Shaker A, Ossaimee R, Salem M, Abouelatta M. A comprehensive semi-analytical model of the polysilicon emitter contact in bipolar transistors. Journal of Computational Electronics 2018; 17: 246-255.

[3] d'Alessandro V, Sasso G, Rinaldi N, Aufinger K. Influence of scaling and emitter layout on the thermal behavior of toward-THz SiGe:C HBTs. IEEE Transactions on Electron Devices 2014; 61: 3386-3394.

[4] Zilak J, Koricic M, Suligoj T, Mochizuki H, Morita S. Impact of emitter interface treatment on the horizontal current bipolar transistor (HCBT) characteristics and RF circuit performance. In: IEEE 2015 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM); Boston, MA, USA; 2015. pp. 31-34.

[5] Stein F, Huszka Z, Derrier N, Maneux C. Extraction procedure for emitter series resistance contributions in SiGe:C BiCMOS technologies. In: Proceedings of 27th International Conference on Microelectronic Test Structures; Udine, Italy; 2014. pp. 20-23.

[6] Krause J, Schroter M. Methods of determining the emitter resistance in SiGe HBTs: a review and an evaluation across technology generations. IEEE Transactions on Electron Devices 2015; 62: 1363-1374.

[7] Kempf PHG. Industry examples at the state-of-the-art: Jazz. In: Cressler JD (editor). Fabrication of SiGe HBT BiCMOS Technology. Boca Raton, FL, USA: CRC Press; 2007. pp. 8-12.

[8] Nicolai M, Zanuccoli M, Fiegna C. Analysis of silicon solar cells with poly-Si/SiOx carrier-selective base and emitter contacts. IEEE Journal of Photovoltaics 2018; 8: 103-109.

[9] Peibst R. From PERC to Tandem: POLO- and p+/n+ Poly-Si tunneling junction as interface between bottom and top cell. IEEE Journal of Photovoltaics 2019; 9: 49-54.

[10] Nemeth B, Young D, Page M, LaSalvia V, Johnston S et al. Polycrystalline silicon passivated tunneling contacts for high efficiency silicon solar cells. Journal of Materials Research 2016; 31: 671-681.

[11] Kunz VD, de Groot CH, Hall S, Ashburn P. Polycrystalline silicon-germanium emitters for gain control, with application to SiGe HBTs. IEEE Transactions on Electron Devices 2003; 50: 1480-1486.

[12] Tilke AT, Forster M, Schupke K, Freigofas A, Wagner C et al. As-doped polysilicon emitters with interfacial oxides and correlation to bipolar device characteristics. Journal of Vacuum Science and Technology B 2005; 23: 1877-1882.

[13] Yu Z, Ricco B, Dutton R. A comprehensive analytical and numerical model of polysilicon emitter contacts in bipolar transistors. IEEE Transactions on Electron Devices 1984; 31: 773-784.

[14] Chu KM, Pulfrey DL. An improved analytic model for the metal-insulator-semiconductor tunnel junction. IEEE Transactions on Electron Devices 1988; 35: 1656-1663.

[15] Ricco B, Stork JMC, Arienzo M. Characterization of non-ohmic behavior of emitter contacts of bipolar transistors. IEEE Electron Device Letters 1984; 5: 221-223.

[16] Linder M, Ingvarson F, Jeppson KO, Grahn JV, Zhang SL et al. Extraction of emitter and base series resistances of bipolar transistors from a single DC measurement. IEEE Transactions on Semiconductor Manufacturing 2000; 13: 119-126.

[17] Gabl R, Reisch M. Emitter series resistance from open-collector measurements—influence of the collector region and the parasitic pnp transistor. IEEE Transactions on Electron Devices 1998; 45: 2457-2465.

[18] Morizuka K, Hidaka O, Mochizuki H. Precise extraction of emitter resistance from an improved floating collector measurement. IEEE Transactions on Electron Devices 1995; 42: 266-273.

[19] Hu C. Modern Semiconductor Devices for Integrated Circuits. Englewood Cliffs, NJ, USA: Prentice Hall, 2010.

[20] Schuegraf KF, Hu C. Modeling hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation. IEEE Transactions on Electron Devices 1994; 41: 761-767.

[21] Lee WC, Hu C. Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence-band electron and hole tunneling. IEEE Transactions on Electron Devices 2001; 48: 1366-1373.

[22] Ohmi T, Isagawa T, Kogure M, Imaoka T. Native oxide growth and organic impurity removal on Si surface with ozone-injected ultrapure water. Journal of the Electrochemical Society 1993; 140: 804-810.

[23] Josquin WJ, Boudewijn PR, Tamminga Y. Effectiveness of polycrystalline silicon diffusion sources. Applied Physics Letters 1983; 43: 960-962.

[24] Lenzlinger M, Snow EH. Fowler-Nordheim tunneling into thermally grown SiO_2. IEEE Transactions on Electron Devices 1968; 15: 686-686.

[25] Miranda E, Palumbo F. Analytic expression for the Fowler–Nordheim V–I characteristic including the series resistance effect. Solid-State Electronics 2011; 61: 93-95.

[26] Fischer A, Mousa M, Forbes R. Influence of barrier form on Fowler–Nordheim plot analysis. Journal of Vaccum Science Technology B 2013; 31: 032201.

[27] Sze SM, Ng KK. Physics of Semiconductor Devices. 3rd ed. Hoboken, NJ, USA: John Wiley and Sons; 2007.

[28] Tsou BPC, Chu KM, Pulfrey DL. Series resistance calculations for polysilicon tunnel junction emitter transistors. Canadian Journal of Physics 1989; 67: 218-220.