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An efficient reliability simulation tool for lifetime-aware analog circuit synthesis

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Abstract: Time-dependent degradation (aging) has become more severe in modern CMOS technologies. Therefore, it is highly critical to capture the variation effects and design reliable circuits against aging. Simulation of time-dependent variations is quite complicated since the degradation is a function of time, where the step count of simulation directly affects the accuracy and the efficiency of the analysis. Commercial simulator tools use a constant step count during reliability simulations, in which choosing a large step count degrades the efficiency whereas keeping it small may result in accuracy problems. To overcome this bottleneck, a couple of different approaches have been proposed in the literature. Nevertheless, they suffer from the initial workload during step count determination and some other accuracy problems. In this study, a two-level step count determination approach is presented, in which the step count induced estimation error can be promptly determined via an effective simulation strategy at the first level. At the second level, the error is fitted into a saturated power law model; thus, the efficient step count can be determined without any simulation effort. To demonstrate the developed tool, two case study circuits have been designed using 130 nm technology parameters. According to the simulation results, the proposed approach decreases the initial workload by up to 67%. The proposed approach provides a remarkable save in computation time and can be used for all analog circuits without loss of generality. Moreover, a reliability-aware analog circuit synthesis tool is implemented to demonstrate the efficiency of the proposed approach. The developed tool provides a 37% improvement in the computation time compared to the only tool in the literature.

Key words: Reliability, aging, simulation, CAD, EDA, analog, synthesis

1. Introduction

CMOS analog circuits suffer from several time-independent and -dependent variability problems. The adverse effect of such problems on circuit performances has been risen due to aggressive and continuous down-scaling of feature size, where both process tolerances during fabrication and local electrical and thermal stresses on devices have worsened along with downscaling of devices [1, 2]. Process, voltage, and temperature (PVT) variations are the well-known time-independent variability problems, which have been studied for many years and numerous accomplished models, efficient simulation techniques, and circuit design approaches robust to PVT variations have been developed. Moreover, during the last decade, analog design automation tools have been replaced by sophisticated ones that take PVT into account; hence, they have become capable of synthesizing robust circuits against process variations [3–5].

The case for the time-dependent degradation mechanisms is quite different. First, modeling of aging mechanisms is more complicated due to the time-dependency. Since it would be highly inefficient to measure

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the aging effects under nominal conditions, semiempirical aging models are constructed via the acceleration aging tests (AAT) [6–8]. Second, simulation of time-dependent degradation mechanisms is another challenging problem. Namely, aging mechanisms such as hot carrier injection (HCI) and bias temperature instability (BTI) cause an increase in the threshold voltage over time, where the change in V_{th} is a function of time (t), channel length (L), temperature (T), and the drain-source (V_{DS}) and gate-source (V_{GS}) voltages [9, 10]. Among all these variables, transistor terminal voltages change over time so that the stress conditions continuously change. Therefore, one-step reliability simulation results in inaccurate lifetime estimations. To overcome this problem, the stress conditions are updated within certain periods (time step lengths) during aging simulations. Conventionally, the total simulation time is divided into subperiods by a certain step count in commercial tools such as MOSRA (Synopsys) [11], UDRM (Mentor) [12], and RelXpert (Cadence) [13]. However, using a constant step count may lead to a demanding trade-off between the accuracy and the efficiency of the analysis.

As illustrated in Figure 1, choosing a small step count or longer time step length may result in inaccurate estimations whereas keeping the step count larger may cause a dramatic increase in the computation time. This problem becomes very critical especially for reliability-aware design automation tools [14, 15]. During the synthesis process, the optimizer visits several thousands of solution points, in other words, an excessive number of simulations are performed. As a result, the synthesis time exponentially increases when the reliability analysis is included to the conventional optimization flow. Therefore, the computation cost (initial workload + number of simulations) should be minimized to keep the synthesis time within practical limits.

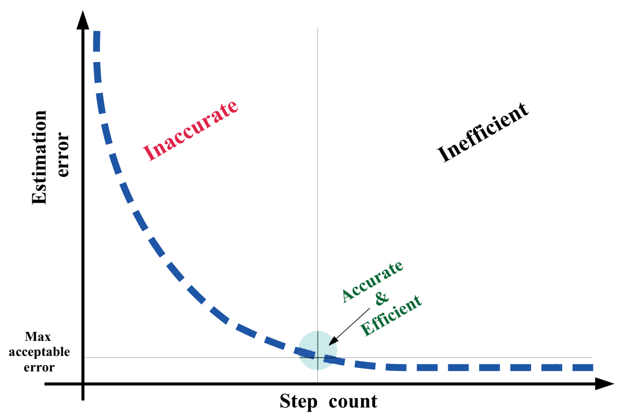

Figure 1. Estimation error is highly correlated with (inversely proportional to) the simulation step count.

This study proposes a novel step count determination approach and an aging simulation tool. The proposed approach consists of three levels. At the first level, a projection of estimation error is obtained with an efficient strategy by running just a few simulations. At the second level, the obtained error data is fitted into a model and the efficient step count is determined by using the model without running any simulations. At the last level, reliability simulation is performed by using the determined step count. To demonstrate the efficiency of the tool, two analog circuits were designed and simulated with the proposed tool. Furthermore, the proposed tool was also integrated with an analog circuit optimizer to reveal the impact of the tool on the synthesis process.

Remainder of the paper is as follows. In Section 2, the related work in the literature is briefly discussed and the main contribution of this paper is highlighted. In Section 3, the proposed step count determination approach and the aging simulator are introduced and explained in detail. Also, the case study circuits and simulation results are provided and discussed. The developed reliability aware circuit synthesis tool is presented and the contribution of the proposed aging simulation on the synthesis time is demonstrated in Section 4. Finally, the paper is concluded in Section 5.

2. Related work and contributions

Commercial aging simulators use a constant step count, where the user determines the step count at the beginning and the total simulation is divided into subperiods. However, this is an inconvenient way to simulate aging effects, which may result in either waste of computation time or inaccurate estimations. To solve this problem, a couple of different step count determination approaches have been proposed in the literature [16–18].

In [16], the step count is dynamically determined by considering the variation on the circuit performances at each time step. The next step count is determined by using a formula when any considerable change occurs in the performance; otherwise, the simulation proceeds with the former step count. In this approach, unlike the discussion in [17], the accuracy has the priority over the efficiency since the change in the performance is considered rather than the change in the transistor parameters. Even though the claim in [17] was missing of some important stress condition updates, that is not the fact. Actually, considering V_{th} change may result in misevaluation since even small changes in transistors' parameters may degrade the circuit performance due to nonlinear nature of analog circuits. Furthermore, being out of transistors' nominal operation regime will directly affect the circuit performance, so such a change can also be captured via performance based evaluation.

Two adaptive step count approaches are presented in [17]. In the first approach, the step count is dynamically determined considering the time to update stress conditions, where the critical value for acceptable variation is determined by the user. In the second approach, a fixed number of step count is allowed and distributed over time. One step calculation is performed for the whole circuit and the transistor exposed to worst case degradation is only considered. The allowable variation is determined with dividing this worst case degradation by the fixed step count. In both approaches, the decision to update time is made by considering the variation in the V_{th}, which may result in accuracy problems as aforementioned. Furthermore, no simulation is performed at each intermediate step to avoid computation workload; however, this may lead to accuracy problems in some applications.

Another step count determination approach is presented in [18]. Unlike the approaches proposed in [17], the efficient step count is determined via SPICE simulations, in which an initial phase of the lifetime is used for the step count determination. Here, this initial phase is evaluated as the whole lifetime duration, where a reliable simulation is performed by using a relatively large step count. Then, the same simulation is repeated for different step counts starting from the minimum number. Finally, the efficient step count is determined considering the estimation error between the reliable and the instant simulations. This loop ends when the error decreases to a predetermined level and the last step count value is used for the remaining lifetime simulation. However, the number simulations performed at the initial phase may degrade the time efficiency due to the repeated considerations of the same time duration.

Analog circuit design tools have become more pronounced over the last two decades. Moreover, these tools have been modified by including variability analysis to the performance evaluation; thus, it is possible to synthesize robust circuits against process variations. The case for reliability-aware synthesis is similar, for which the variability analysis is replaced by an aging simulation. However, one further challenge arises during the augmentation of the optimizer with aging analysis. Considering the numerous iterative evaluations during the optimization process, using an expensive aging simulator in terms of computation time degrades the time efficiency of the synthesis. Even though several yield-aware analog circuit sizing tools have been developed in the literature [19–21], there is only one published lifetime-aware analog circuit synthesis tool [14], which employs the aging simulator proposed in [18] is employed. To enhance the synthesis time, infeasible solution elimination is called during optimization process. However, the approach suffers from the initial workload during step count determination, which degrades the time efficiency.

Main contributions of this study are as follows:

- An efficient step count determination approach for aging simulations was proposed. By using the proposed approach, an analog circuit aging simulator with dynamic step count was developed, which considerably improves the efficiency of the reliability simulations keeping the accuracy at a certain level.
- To demonstrate the proposed approach and developed the tool, two amplifier circuits (a single stage amplifier and a folded cascode amplifier) were designed and simulated.
- The developed tool provides a remarkable save in computation time (up to 67%) and can be used for all analog circuits without loss of generality. To adapt the tool for other technologies, the only modification would be replacing ad hoc aging models. Once a model is generated, the efficient step counts for different accuracy levels can be determined without performing additional simulations.
- The developed simulator was also embedded into an analog circuit synthesis tool [22] and a reliability-aware analog circuit synthesis tool was implemented. According to the results, a 37% improvement was achieved in the computation time.

3. The proposed work: reliability simulation tool with efficient step count determination

Among several degradation mechanisms, hot carrier injection (HCI) and bias temperature instability (BTI) have been reported as the major problems that cause aging in CMOS circuits.

HCI occurs when the carrier energy level achieves a certain high value near the drain region. These accelerated carriers lead to impact ionization above the pinch-off region, which results in an electron-hole pair. Generated electrons get trapped into the oxide and create interface states. Traps cause an increase in the threshold voltage and may reduce the channel mobility due to scattering along the channel [23]. Conventionally, it has been assumed that HCI is negligible in p-channel devices due to lower hole mobility. The degradation in I_d resulting from HCI is modeled by Equation 1.

$$\Delta I_d = I_d.A.{V_{ds}}^{p_1}.e^{\frac{-E_a}{kT}}.L^{p_2}.t^{p_3} \tag{1}$$

A, p_1, p_2 are technology dependent device parameters, k is the Boltzmann constant, T is temperature, L is the transistor channel length, V_{ds} is the drain-source voltage, E_a is the activation energy, t is time, and p_3 is the time exponent [8].

On the other hand, NBTI occurs due to the high electrical field across the gate oxide, where preexisting interface states catch carriers, trap them for a certain time, and later release them back into the channel. Filled interface states shift the threshold voltage of the device. Removal of stress can recover some of the interface traps and result in partial relaxation [24]. The consequence of NBTI on PMOS transistor is the increase in the threshold voltage, which is modeled as given in Equation 2.

$$\Delta V_{th} = B.\left(V_{gs}\right)^{m_1}.e^{\frac{-E_a}{kT}}.L^{m_2}.W^{m_3}.t^{m_4} \tag{2}$$

where, B, m_1, m_2, m_3 are technology dependent fitting parameters, W is the transistor channel width, and m_4 is the parameter depending on the hydrogen passivation process during fabrication.

The proposed approach is based on extracting error trajectory by performing simulation with different step counts; thus, an error model is obtained for each design under test (DUT) circuit. A simulation based aging simulator, whose pseudo-code is given in Algorithm 1, is realized in this study. The aging simulation starts with a fresh simulation to obtain the prior stress conditions (V_{ds} and V_{gs} values). By using this data, degradation amount of each device is calculated via Equation 1 and Equation 2. Then, the transistor model files (Model Cards) are updated and aging simulation is performed for $T_{age} = T_{final}/N_{step}$, where T_{age}, T_{final}, and N_{step} denote the simulation time per step (e.g., 1 year), the total lifetime simulation (e.g., 10 years), and the step count (e.g., 10), respectively. This loop is repeated until $T_{final} = T_{age}$.

Algorithm 1: Pseudo-code of the aging simulation flow.

```
Input: t_final, N_step;
Δt = 0, ΔV_th1,2,...m = 0, k = 1;
(S(1,:), F(1,:)) ⇐ simulation_fresh();
while t_step < t_final do
    k++;
    Δt = Δt + t_final/N_step;
    ΔV_th1,2,..,m = Degradation(S_k-1,p, t_step);
    (ModelCards) ⇐ Update(ΔV_th1,2,..,m);
    (S(k,:), F(k,:)) ⇐ simulation_age();
end
return S, F
```

A general flow of the proposed reliability simulation approach is provided in Figure 2. The proposed approach involves 2 different phases. The first phase starts with initial description of simulation duration (T_{final}), the initial step count ($N_{initial} = 2$), and the allowable degradation error in the worst case circuit performance (ϵ_{allow}). $N_{initial}$ is chosen as 2 in order to obtain common intercept points between the iterations. The first aging simulation is performed with these initial parameters to obtain the first reference point. As the next step, the simulation duration is halved by keeping $N_{initial} = 2$ and the aging simulation is called again. Here, it should be noted that dividing the time duration by two means increasing the step count in a logarithmic manner since the time to maximum allowable error is looked for. The relative error is calculated for circuit performances of the final point for the last and the midpoint of the former analysis. Then, the calculated error (ϵ_i) is compared with the maximum allowable error, where if (ϵ_i) is greater than ϵ_{allow}, one more simulation is performed by dividing the time duration by 2 (multiplying N_{step} by 2). This procedure is visually illustrated in Figure 3. Let us consider a 10 years simulation. At first, the total time is divided by $N_{initial} = 2$, so there will be data for 5 and 10 years for this initial simulation. Then, the total time is divided by 2 again; hence, we will have 2.5 and 5 years aging data. In the next step, the error is calculated according to the difference between the first 5 years (one-step) and the second 5 years (two-steps) data. This iteration is repeated until the error is less than the targeted error tolerance. Otherwise, the calculated error data is transmitted to the modeling part, in which the error points are fitted into a model. The saturated power-law model given in (3), where a and b are model coefficients, is used during the modeling phase. The idea behind using such a model is due to the saturated nature of aging. Namely, a large portion of the degradation occurs during the initial period of the total lifetime since the number of interface states (traps) decrease over time [14]. Hence, the change in the threshold voltage becomes insignificant and does not cause any considerable change in the biasing points. Therefore, updating the bias voltages does not provide any improvement after a certain time.

$$N_{step} = a(1+\epsilon_{allow})^b \tag{3}$$

Here, one should consider that the last step count value is not the most appropriated one since the step count is increased in a logarithmic manner, where the distance between the last two consecutive step count values may be relatively large. Therefore, a more suitable step count is a value between the last and the one former points, which can be easily obtained from (3) without any additional simulation. Once the model is generated, the corresponding step count for a certain accuracy level can be immediately obtained. This feature may facilitate the lifetime-aware optimization by determining the accuracy level similar to simulated annealing; thus, the computation time can be saved substantially.

To demonstrate the proposed approach, a single stage amplifier, whose schematic is shown in Figure 4, was designed at 130 nm CMOS technology.

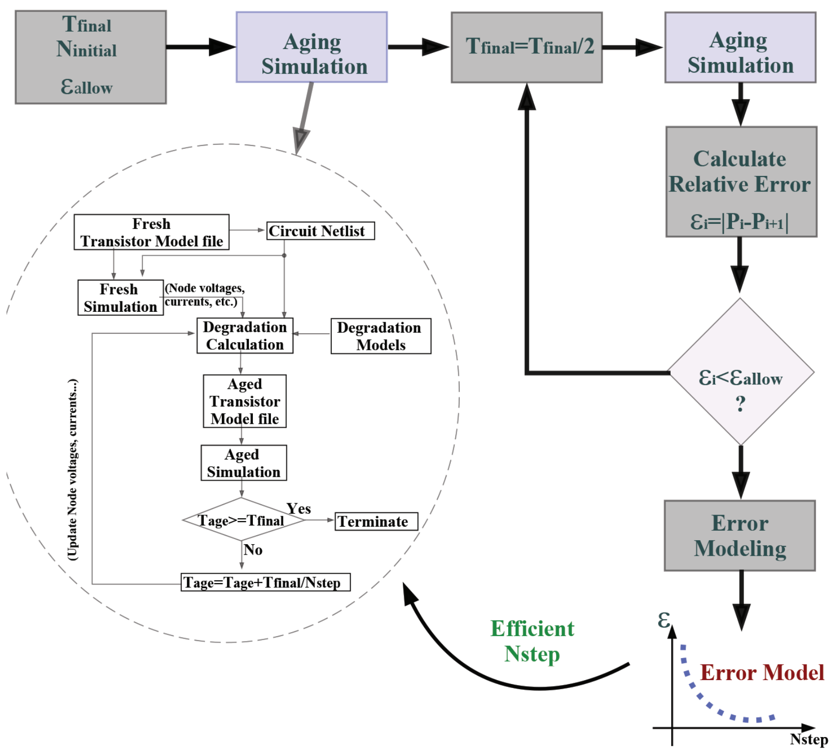

Figure 2. A general flow of the proposed approach.

The obtained relative error in the gain of the amplifier is provided in Figure 5. The ϵ_{allow} was selected as 1%, in other words, the simulation phase is stopped when the estimation error in the worst case performance metric, that is the dc gain for this circuit, is less than 1%. As seen from the figure, the relative error decreases to 1% somewhere between 64 and 128. However, the simulation data has two points there and it is impossible to determine that point. Here, the model takes the role and accurately localizes the optimal point ($N_{step} = 82$)

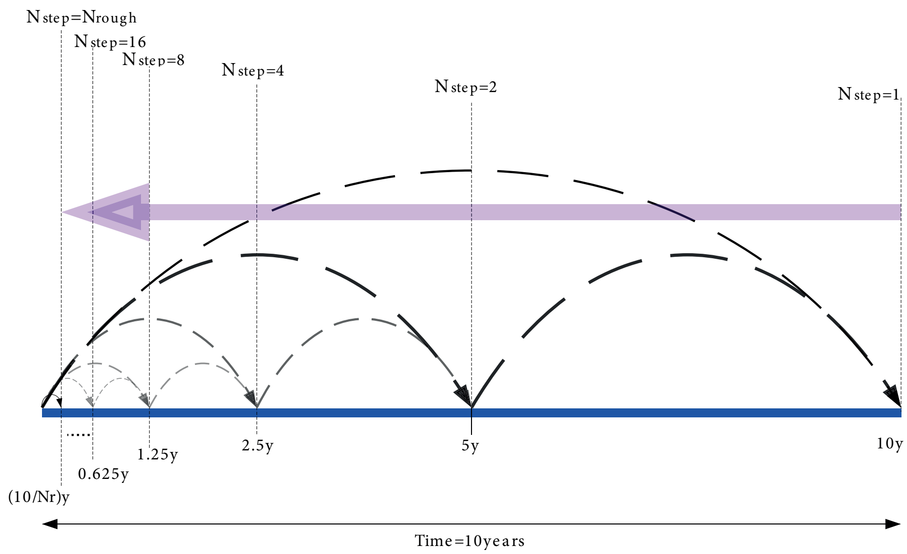

Figure 3. An illustration of the step count determination approach.

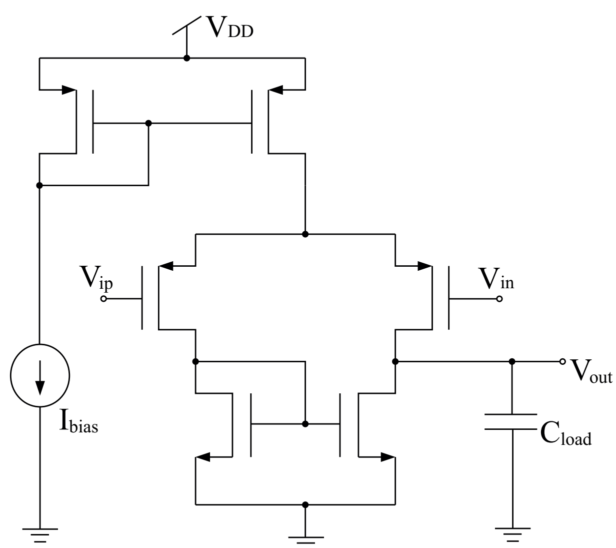

Figure 4. The schematic of the single stage amplifier.

without any simulation effort. A list of accuracy levels for different step counts is provided in Table 1. The initial workload for this example is only 12, whereas the proposed simulators in [17] and [18] allocate much more budget at the beginning to determine the efficient step size. Furthermore, the designer has the flexibility to determine the accuracy level by only changing the ϵ_{allow} without performing any additional simulation in the proposed approach while one should perform additional simulations in the other tools.

As the second example, a folded cascode amplifier given in Figure 6 was designed using 130 nm CMOS technology parameters. The open-loop gain, the 3dB bandwidth, and the phase margin were considered as the major design performances. According to the fresh simulation results, design performances were measured as $62dB$, $65kHz$, and 55^o, respectively. User defined variables, t_{final}, $N_{initial}$, and ϵ_{allow} were determined as 10 years, 2, and 1%, respectively.

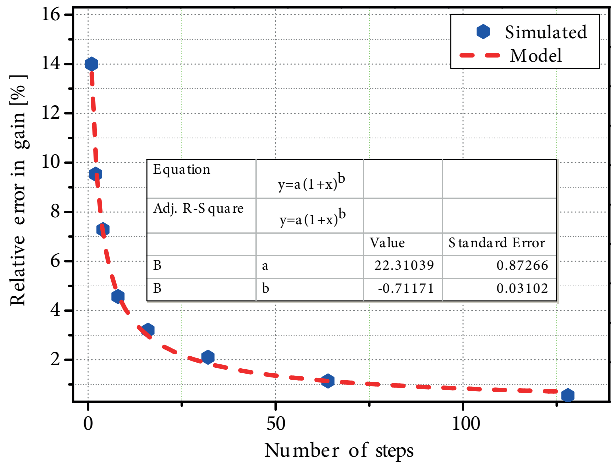

Figure 5. Estimation error vs number of steps.

Table 1. Accuracy level vs Step count.

Accuracy level (E_{allow})	Step count (N_{step})
0.1%	198
1%	82
3%	21
5 %	8

Threshold voltage degradation results for the worst case device are given in Figure 7. According to the results, as expected, the estimation error considerably decreases along with increasing step counts. The estimation error of the determined step count is 0.7% at the end of the lifetime simulation (10 years). The response of the circuit to this error is provided in Figure 8, which is also used in the step count decision mechanism. The estimation error was found 0.95%. To demonstrate the efficiency of the tool, 3 different solutions for the folded cascode amplifier circuits were simulated by using the proposed tool and the tool presented in [18]. Table 2 provides the comparison results. As can be seen from the table, the proposed work provides a remarkable decrease in the initial simulation work, which ultimately results in a save in the simulation time up to 67% without any loss in the accuracy. This save shoots up when the proposed aging simulator is used in the automatic synthesis of robust circuits, where reliability simulations are performed for several hundreds, even thousands. The circuit was simulated by using both the fixed step count approach ($N_{step} = 10,\ 20,\ 50,$ and 1000) and the proposed approach. The efficient step count was estimated as 162 by the proposed approach, where 14 initial simulations were performed.

4. Reliability-aware analog circuit synthesis tool

A reliability-aware analog circuit sizing tool was implemented by integration of the proposed aging simulation tool and a single-objective optimization engine. A general flow chart of the developed tool is given in Figure 9.

The developed tool is an improved version of the tool presented in [14]. To improve the synthesis time, the aging simulator was replaced by the tool developed in this work. To move the efficiency one step further, the accuracy level of aging simulation is dynamically determined rather than a fixed accuracy level.

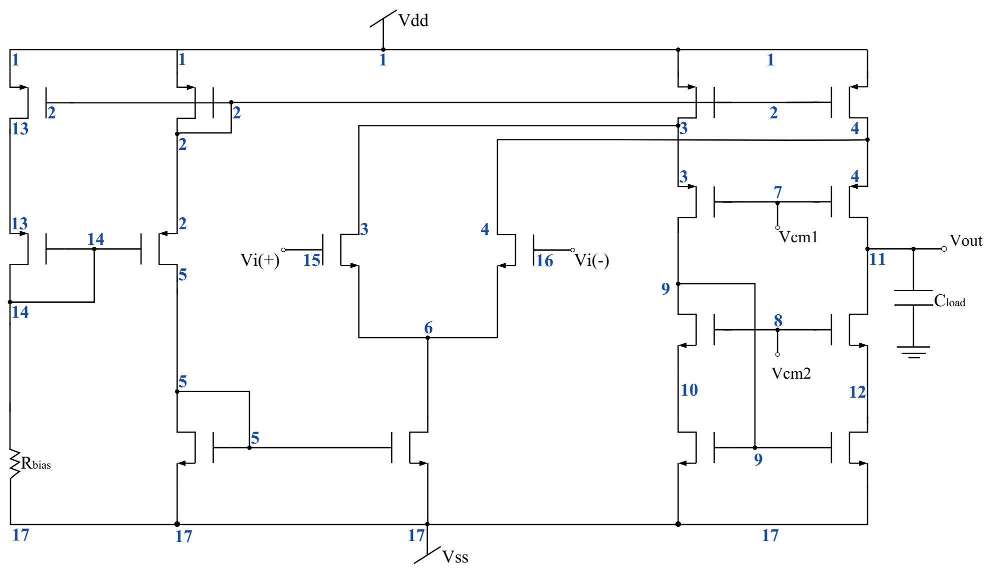

Figure 6. Schematic of the folded cascode amplifier.

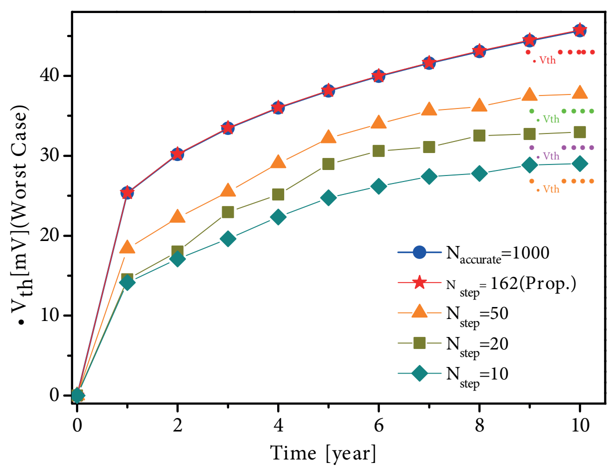

Figure 7. V_{th} degradation for different step counts.

Table 2. Comparision results.

		N_{step}	$N_{accurate}$	Initial work [# of sim.]	$\epsilon_{\Delta V_{th}}$ [%]	$\epsilon_{f_{3dB}}$ [%]	Time [s]
This work	DUT-1	89	1000	12	1.02	0.9	86
	DUT-2	123	1000	12	1.2	0.84	115
	DUT-3	135	1000	14	0.95	0.45	130
Proposed tool in [18]	DUT-1	100	1000	50	0.85	0.95	128
	DUT-2	140	1000	78	0.96	1.4	194
	DUT-3	160	1000	84	0.78	1.2	208

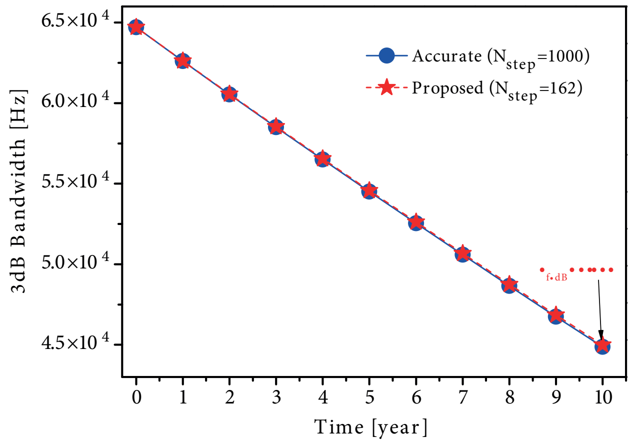

Figure 8. 3dB bandwidth reliability simulation results.

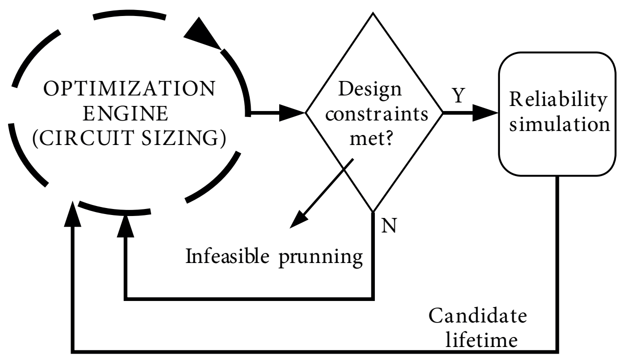

Figure 9. A general flow chart of the reliability aware analog circuit synthesis tool.

The optimization engine uses an evolutionary strategies (EA) algorithm during solution search and a simulated annealing (SA) algorithm during the selection process. The single objective is called as *cost*, which is the sum of distances of the design specifications to the targeted values. The evaluation process is carried out by SPICE simulations. The optimization starts with the creation of the first generation and mimics the evolution theory, which includes cross-over, mutation, and selection (determining of the survived individuals) operations through the generations. The optimization is ended either the convergence or the maximum number of iterations is achieved. Further details can be found in [22].

An infeasible pruning mechanism is employed to select individuals who satisfy the design constraints with a certain level. This level is called as acceptance region, where the boundaries are decided according to the user-defined coefficients. Candidates satisfying the acceptance region criteria deserve reliability simulation; thus, redundant simulations are avoided for infeasible solutions. The size of the acceptance region directly affect the optimization efficiency, where enlarging the region results in excessively increased synthesis time due to raised expensive reliability simulations. On the other hand, one should consider that keeping the region small may cause missing of some solutions that slightly violate the design constraints, but reliable ones. One important novelty of this version is that the infeasible pruning is activated after a certain number of iterations passed in order to let population get matured whereas it is applied to all populations in [14].

As previously discussed, the maximum allowable error (ϵ_{allow}) is the critical parameter that should be minimized to obtain a certain accuracy in the lifetime estimation. However, choosing it unnecessarily small may result in excessively increased simulation time. Considering the numerous iterations in the optimization process, the increase in the computation time may be far beyond the expectation. To palliate this bottleneck, a new decision mechanism is included to the optimization engine, in which the ϵ_{allow} is decided according to a Metropolis criterion. Since the convergence is relatively far at the beginning, an exact estimation of the lifetime is not necessary at this phase. Therefore, the ϵ_{allow} can be kept at small to save the computation time. Then, it is increased along with the generations. The idea behind the decision mechanism is based on arranging the ϵ_{allow} considering a variable called population temperature. The temperature is determined high (1000) at the beginning and decreases as optimization proceeds. As the temperature decreases, the ϵ_{allow} is also decreased to improve the estimation accuracy for matured solutions. Hence, the step count can be kept small for immature populations whereas higher values are assigned to individuals close to the convergence.

A basic 2 stage OTA shown in Figure 10 was chosen as the synthesis example, which has 24 independent design parameters (transistor dimensions, bias resistor, and compensation capacitor). The design boundaries are listed in Table 3. The acceptance region coefficients for infeasible pruning were determined as $7.2kHZ$ bandwidth, $63dB$ gain, and 54^o phase margin. The limits of design constraints for lifetime calculation were determined as $7kHz$ bandwidth, $60dB$ gain, and 50^o phase margin, respectively.

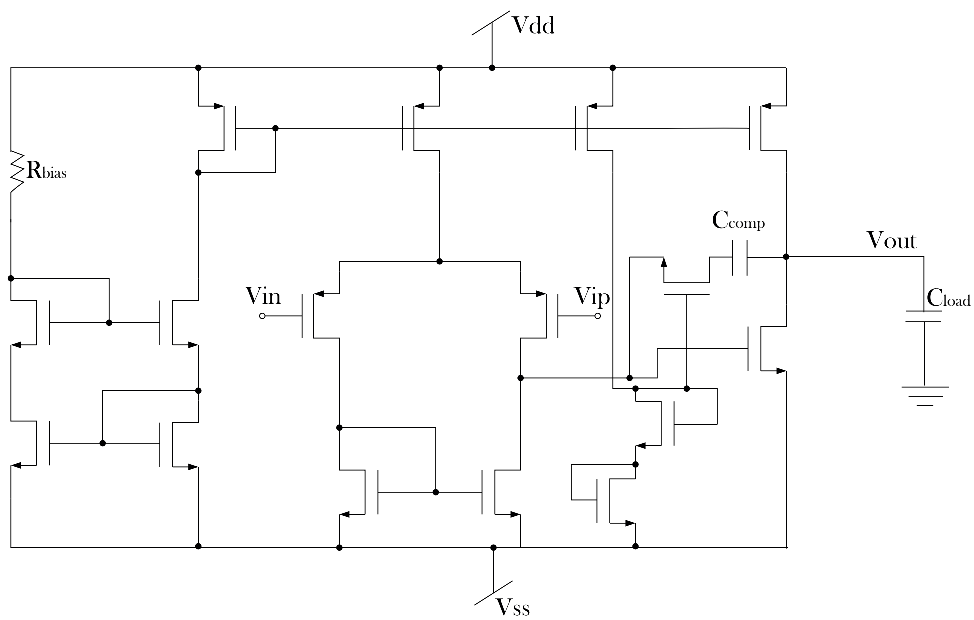

Figure 10. The schematic of a basic 2 stage OTA.

Table 3. Design boundaries and variables for 2 stage OTA.

W $[\mu m]$	L $[\mu m]$	R_{bias} $[\Omega]$	C_{com} $[pF]$	V_{dd} $[V]$	V_{ss} $[V]$	C_{load} $[pF]$
0.65-130	0.12-10	100-10000	0.1-50	1.2	0	0.5

The 2 stage OTA circuit was synthesized with the developed tool and results for 3 independent runs are provided in Table 4. Synthesis results generated by the tool in [14] are also provided for comparison. Considering the design constraints, both tools can find satisfied solutions in terms of electrical specifications. Violations in

Table 4. Synthesis results of 3 independent runs for 2 stage OTA.

Design constraints		Bandwidth [$> 10kHz$]	Gain [$> 70dB$]	Phase margin [$> 50^o$]	Power [$< 1mW$]	Area [$< 1500\mu m^2$]	Lifetime [$> 5years$]	Synthesis time [$min.$]
This work	1	10.6	72.11	65	1.4	2285	6.16	29.6
	2	11	70.54	68	1.4	2368	7.82	30.2
	3	12	70.12	64	1.3	2850	6.54	32.1
The tool proposed in [14]	1	11.5	71.34	67.14	1.3	2370	6.25	44.6
	2	15.9	70.16	64.3	1.4	2700	5.75	46.8
	3	13.4	70.10	70.42	1.5	2620	7.5	49.53

power and area are the results of lifetime-aware synthesis, where the optimizer tends to find solutions more robust; thus, circuits with larger transistors and higher currents were preferred. Considering the lifetime estimations, the proposed tool provides sharper lifetime estimation thanks to the step count determination mechanism. The average synthesis time for the proposed tool is around 30 min whereas it was obtained as 47 min for the other tool. According to the average synthesis time results, the computation effort was reduced by 35% in the proposed tool.

5. Conclusion

This study proposes an efficient and reliable approach to determine the efficient step count for reliability simulations. To increase the reliability, the efficient step count is determined via SPICE simulations, in which degradation in performance specifications are considered rather than the V_{th} degradation. Furthermore, to increase the efficiency, a two-phase step count determination approach was constructed. At the first phase, estimation errors are obtained via SPICE simulations by increasing the step count in a logarithmic manner. At the second phase, these errors are fitted into a saturated power-law model; thus, the efficient step count is determined according to the accuracy constraint without performing any simulations. The proposed approach can be used for all analog circuits without loss of generality. By using the proposed approach, an aging simulator was developed. Simulation results indicated that the proposed tool provides almost 67% improvement in the computation time. The developed tool was also integrated with a single-objective analog circuit sizing tool, so a novel reliability-aware analog circuit synthesis tool was constructed. Synthesis results demonstrated that the synthesis time can be improved by 37% on average compared to the only lifetime-aware circuit sizing tool in the literature.

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References

[1] Weikang W, Xia A, Xiaobo J, Yehua C, Jingjing L et al. Roughness induced single event transient variation in SOI FinFETs. Journal of Semiconductors 2015; 36 (11): 114001. doi: 10.1088/1674-4926/36/11/114001

[2] Kiamehr S, Weckx P, Tahoori M, Kaczer B, Kukner H et al. The impact of process variation and stochastic aging in nanoscale VLSI. In: IEEE International Reliability Physics Symposium; Pasadena, CA, USA; 2016. pp. CR-1.

[3] Canelas A, Póvoa R, Martins R, Lourenço N, Guilherme J et al. FUZYE: A fuzzy C-means analog IC yield optimization using evolutionary-based algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2018; 39 (1): 1-13.

[4] De Lima Moreto RA, Thomaz CE, Gimenez SP. Automatic optimization of robust analog CMOS ICs: An interactive genetic algorithm driven by human knowledge. In: 31st IEEE Symposium on Integrated Circuits and Systems Design; Rio Grande do Sul, Brazil; 2018. pp. 1-6.

[5] Kondamadugula S, Naidu SR. Variation-aware parameter based analog yield optimization methods. Analog Integrated Circuits and Signal Processing 2019; 99 (1): 123-32.

[6] Shen CN, Yang XW, Chang C, Chao MC. The study of activation energy (Ea) by aging and high temperature storage for quartz resonator's life evaluation. In: Proceedings of the Symposium on Piezoelectricity, Acoustic Waves and Device Applications; Fujian, China; 2010. pp. 118-122.

[7] Bravaix A, Guerin C, Huard V, Roy D, Roux JM et al. Hot-carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature. In: IEEE International Reliability Physics Symposium; Montreal, Quebec, Canada; 2009. pp. 531-548.

[8] Afacan E, Dündar G, Pusane AE, Başkaya F. Semi-empirical aging model development via accelerated aging test. In: 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design; Lisbon, Potugal; 2016. pp. 1-4.

[9] Junior NG and Barraud S. Experimental analysis of negative temperature bias instabilities degradation in junctionless nanowire transistors. In: 33rd Symposium on Microelectronics Technology and Devices; Rio Grande do Sul, Brazil; 2018. pp. 1-4.

[10] Thareja G, Lee J, Thean AV, Vartanian V, Nguyen B. NBTI reliability of strained SOI MOSFETs. In: International symposium for testing and failure analysis; Austin, Texas, USA; 2006. pp. 423-426.

[11] Tudor B, Wang J, Sun C, Chen Z, Liao Z et al. MOSRA: An efficient and versatile MOS aging modeling and reliability analysis solution for 45nm and below. In: 10th IEEE International Conference on Solid-State and Integrated Circuit Technology; Shanghai, China; 2010. pp. 1645-1647.

[12] Graphics SM. Reliability simulation in CMOS 90nm design using Eldo. Wilsonville, Oregon, USA: Mentor, 2009.

[13] Keith G, Mu F, Kapila G, Reddy V. Simulation of circuit reliability with RelXpert. Austin, Texas, USA: Cadence, 2005.

[14] Afacan E, Berkol G, Dundar G, Pusane AE, Baskaya F. A lifetime-aware analog circuit sizing tool. Integration, the VLSI journal 2016; 55 (3):349-356.

[15] Ferreira PM, Cai H, Naviner L. Reliability aware AMS/RF performance optimization. Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design. Pennsylvania, United States; IGI Global, 2014.

[16] Maricau E, Gielen G. Analog IC reliability in nanometer CMOS. Berlin, Germany; Springer Science & Business Media, 2013.

[17] Martín-Lloret P, Toro-Frías A, Martín-Martínez J, Castro-López R, Roca E et al. A size-adaptive time-step algorithm for accurate simulation of aging in analog ICs. In: IEEE International Symposium on Circuits and Systems; Baltimore, MD, USA; 2017. pp. 1-4.

[18] Afacan E, Berkol G, Dundar G, Pusane AE, Baskaya F. A deterministic aging simulator and an analog circuit sizing tool robust to aging phenomena. In: Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design; İstanbul, Turkey; 2015. pp. 1-4.

[19] Afacan E, Berkol G, Dundar G, Pusane AE, Baskaya F. An analog circuit synthesis tool based on efficient and reliable yield estimation. Microelectronics Journal 2016; 54 (3): 14-22.

[20] Golanbari MS, Kiamehr S, Ebrahimi M, Tahoori MB. Variation-aware near threshold circuit synthesis. In: Design, Automation, Test in Europe Conference, Exhibition; Dresden, Germany; 2016. pp. 1237-1242.

[21] Canelas A, Martins R, Póvoa R, Lourenço N, Horta N. Yield optimization using k-means clustering algorithm to reduce Monte Carlo simulations. In: 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD); Lisbon, Portugal; 2016. pp. 1-4.

[22] Sönmez ÖS, Dündar G. Simulation-based analog and RF circuit synthesis using a modified evolutionary strategies algorithm. Integration, the VLSI journal 2011; 44 (2): 144-54.

[23] Groeseneken G, Degraeve R, Kaczer B, Roussel P. Recent trends in reliability assessment of advanced CMOS technologies. In: Proceedings of the 2005 International Conference on Microelectronic Test Structures; Leuven, Belgium; 2005. pp.81-88.

[24] Vattikonda R, Wang W, Cao Y. Modeling and minimization of PMOS NBTI effect for robust nanometer design. In: Proceedings of the 43rd annual Design Automation Conference; San Francisco, USA; 2006. pp. 1047-1052.