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Hybrid self-controlled precharge-free CAM design for low power and high performance

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Abstract: Content-addressable memory (CAM) is a prominent hardware for high-speed lookup search, but consumes larger power. Traditional NOR and NAND match-line (ML) architectures suffer from a short circuit current path sharing and charge sharing respectively during precharge. The recently proposed precharge-free CAM suffers from high search delay and the subsequently proposed self-controlled precharge-free CAM suffers from high power consumption. This paper presents a hybrid self-controlled precharge-free (HSCPF) CAM architecture, which uses a novel charge control circuitry to reduce search delay as well as power consumption. The proposed and existing CAM ML architectures were developed using CMOS 45nm technology node with a supply voltage of 1 V. Simulation results show that the proposed HSCPF CAM-type ML design reduces power consumption and search delay effectively when compared to recent precharge-free CAM-type ML architectural designs.

Key words: Content-addressable memory, low power, match-line, precharge-free, search delay

1. Introduction

Content-addressable memory (CAM) compares stored lookup table data against search data parallel within a single clock cycle [1, 2] and returns the address of the matched data through match-line sense amplifier (MLSA). This parallel search scheme of CAM surmounts the software-based search algorithms for all the high-speed applications such as radix tree [3], image processing [4], 5G communication network [5], mobile devices [6], IP routing [7], gray coding [8] and so on. Parallel hardware activity of CAM exhibits high performance, but consumes large power. Hence, designing the CAM for a reduced power consumption and better performance becomes a challenging task. CAM cells arranged in a single row form one CAM word [9]. Each CAM word is connected to a single match-line (ML) as shown in Figure 1. Prior to the search operation, all the MLs are precharged to high voltage [10]. During search operation, only a single word is matched with search word and the corresponding ML needs to hold the charge. All the other mismatched MLs will be discharged. This regular precharging and discharging of MLs consume considerable dynamic power in CAM. Here, we briefly review a few techniques for power reduction of CAM. Many works were reported to reduce the switching power consumption involved in precharging the MLs. Some researchers worked on segmenting the word into subwords. The segments are arranged in parallel and hierarchical architectures in [11] and [12], respectively. The word is divided into master and slave paths in [13]. In [14], CAM word is divided into NAND-type and NOR-type segments. In this design, a match in the first segment activates the second segment conditionally for further

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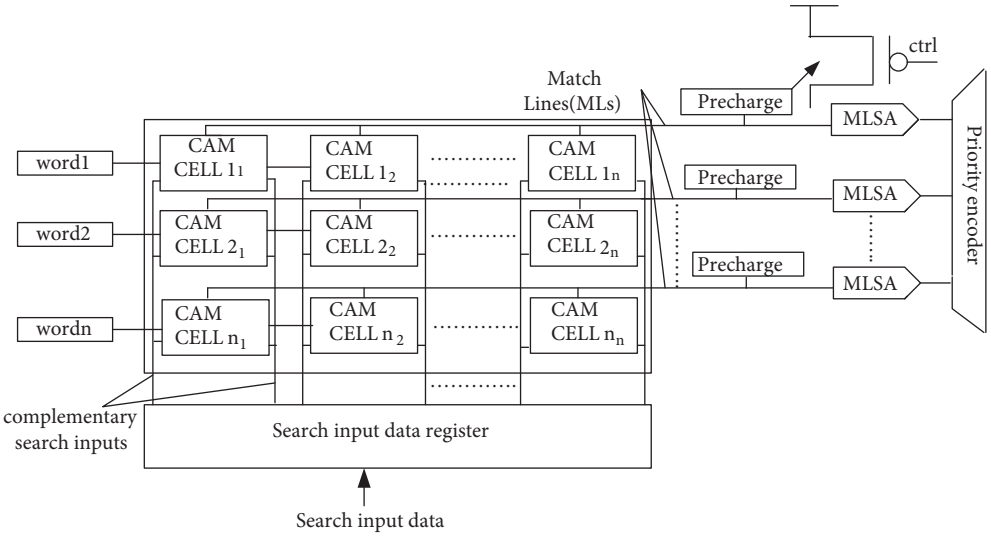

Figure 1. Block diagram of CAM architecture.

search and avoids unnecessary charging and discharging of the second segment even when mismatched. In [15], ML power is reduced by precomputation. Memory organization of precomputation-based CAM (PB-CAM) consists of parameter extractor (PE), CAM memory, and a smaller parameter memory (PM). PE is a circuit which extracts a parameter (one's count of input word) from the input data. The searching operation is done in two parts. Initially, the extracted parameter is compared with the data in PM. The words in the CAM whose parameters are matched will only be activated for further search. As parameter memory is smaller than CAM memory, the comparisons in the first part are smaller. Similarly, in the second part, the comparisons are made only for the matched data. Hence, PB-CAM exploits the reduction in the number of comparisons and thereby reduces power consumption. The authors in [16] addressed the issue of short circuit (SC) power consumption in conventional NOR CAM and developed a precharge-free (PF) CAM which eliminates SC current path during mismatch condition. PF CAM also avoids charge sharing of NAND CAM cell, but it suffers from degraded performance due to a series chain of MLs. To improve the performance of the PF CAM design further, in [17], self-controlled precharge (SCPF) CAM ML, where output control is based on the charge at each CAM cell node, was designed. This design was developed to improve the performance, but at the cost of power consumption. In this paper, we tried to overcome the drawbacks of PF CAM and SCPF CAM by designing a new precharge-free CAM ML architecture, hybrid self-controlled precharge-free (HSCPF) CAM, in which output control is based on the charge at each successive two CAM cell nodes.

The rest of the paper is organized as follows: Section 2 explains traditional CAM match-line architectures. Section 3 explains precharge-free CAM match-line architectures. Section 4 proposes HSCPF CAM. The comparison results of power consumption, search delay, and energy-metric between the proposed and conventional CAM architectures for different Process Corners, Monte Carlo simulations are presented in Section 5, and Section 6 concludes the paper.

2. Traditional CAM architecture

CAM architecture is constructed with an array of memory elements along with comparison circuits. Memory elements can either be volatile or nonvolatile [18]. Generally, 6T static random access memory (SRAM) cell

is used to build the memory [19]. NAND-type and NOR-type ML architectures are the two basic comparison circuits [20].

2.1. NOR match-line CAM architecture

CAM cells are connected in parallel to form NOR ML architecture. Four NMOS transistors are required to design comparison circuitry in NOR CAM cell. Gates of M_1 and M_2 transistors are connected in series to differential storage bits D and D_{bar} of SRAM cell as shown in Figure 2. Gates of transistors M_3 and M_4 are connected to differential search bits SL and SL_{bar}. When precharge control signal $ctrl$ is low, ML precharges to a high voltage through transistor P_1 irrespective of the search input and stored data in the memory. When the $ctrl$ is high during evaluation, the ML output depends on the search input and bits stored in the CAM cells. If all the bits in a row are matched with input search word, then no pull-down path exists for the ML and hence, it retains its precharged value. When the word in a row is not matched with input search word even by one bit, the ML attached to that row will discharge through the pull-down path formed by the mismatched CAM cell. Table 1 shows the truth table of NOR CAM cell for match/miss. NOR ML architecture timing waveform for a miss followed by a match case is shown in Figure 3.

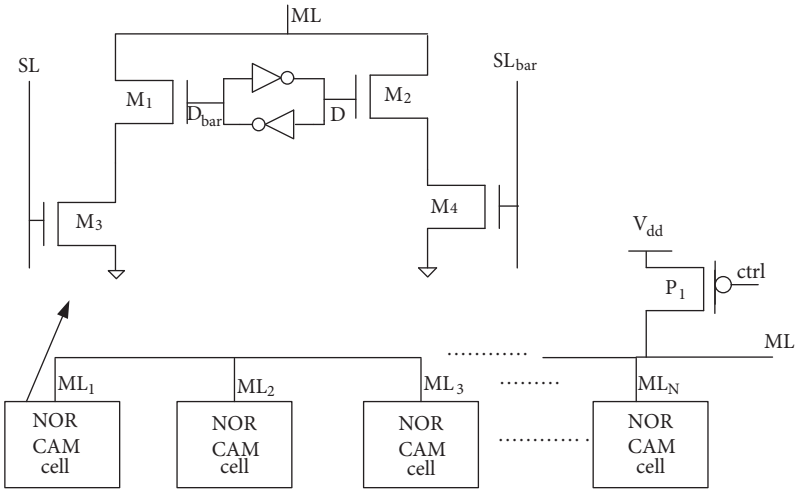

Figure 2. NOR CAM ML architecture.

Power consumption in NOR match-line architecture for a clock cycle is given by Eq. (1):

$$P_{nor} = \alpha_{nor-1} C_{MLnor} V_{DDnor}^2, \tag{1}$$

where α_{nor} = switching activity, C_{MLnor} = ML capacitance, V_{DDnor} = supply.

Delay in NOR ML for a clock cycle is given by Eq. (2):

$$D_{nor} = T_{Dnor} + t_{RCnor}, \tag{2}$$

where D_{nor} = Search delay between ML and ctrl, T_{Dnor} = One transistor delay, t_{RCnor} = ML time constant.

Total time required to complete one clock cycle for NOR ML architecture is given by Eq. (3):

$$T_{NOR} = T_{wr} + T_{pre} + T_{SL}, \tag{3}$$

where T_{NOR} = total time, t_{wr} = write time T_{pre} = precharge time, t_{SL} = evaluation time.

D_{nor} is used to find the search delay between the ML and ctrl signal, whereas T_{NOR} is used to find the amount of time required to complete one operation to indicate ML for miss or match.

Table 1. Truth table for NOR CAM cell.

SL	D	ML	Output indicates
0	0	Match	High
0	1	Miss	Low
1	0	Miss	Low
1	1	Match	High

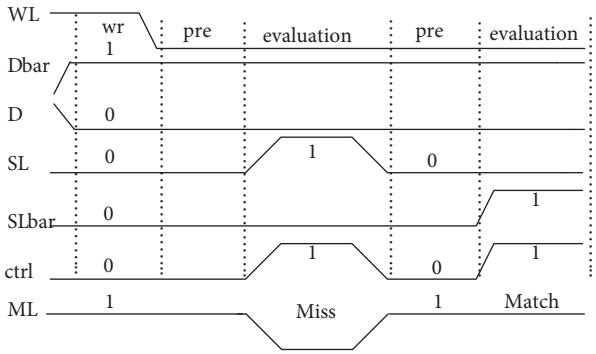

Figure 3. Timing waveform of NOR CAM cell for miss followed by match.

NOR ML CAM architecture offers higher performance but consumes larger power.

2.2. NAND match-line CAM architecture

In NAND ML architecture, CAM cells are connected in series. Three NMOS transistors are required to form comparison circuitry in NAND CAM cell. The gates of M_1 and M_2 transistors are connected in series to complementary storage bits D and D_{bar} as shown in Figure 4. The gate of M_3 transistor is connected to node N. If all the bits in a row are matched with the input search word, then logic 1 is transferred to N nodes of all the CAM cells and the ML attached to that word is connected to ground. If a word in a row is not matched with the input search word, then logic 0 is transferred to node N of all mismatched CAM cells and hence the ML attached to that word starts to charge. In NAND ML architecture, the match indicates low and the miss indicates high. Table 2 shows the truth table of NAND CAM cell for match/miss. NAND ML architecture timing waveform for the match followed by the miss case is shown in Figure 5.

Power consumption in NAND ML architecture for a clock cycle is given by Eq. (4):

$$P_{nand} = C_{MLnand}\ V_{DDnand}^2, \tag{4}$$

Delay in NAND ML for a clock cycle is given by Eq. (5):

$$D_{nand} = N(T_{Dnand} + t_{RCnand}), \tag{5}$$

where N = number of transistors.

Total time required to complete one clock cycle for NAND ML architecture is given by (6)

$$T_{NAND} = T_{wr} + T_{pre} + T_{SL}, \tag{6}$$

where T_{NAND} = total time, t_{wr} = writ time T_{pre} = precharge time, t_{SL} = evaluation time.

NAND ML CAM architecture offers low power consumption but degrades the performance; therefore, NOR ML architecture is preferred over NAND ML architecture.

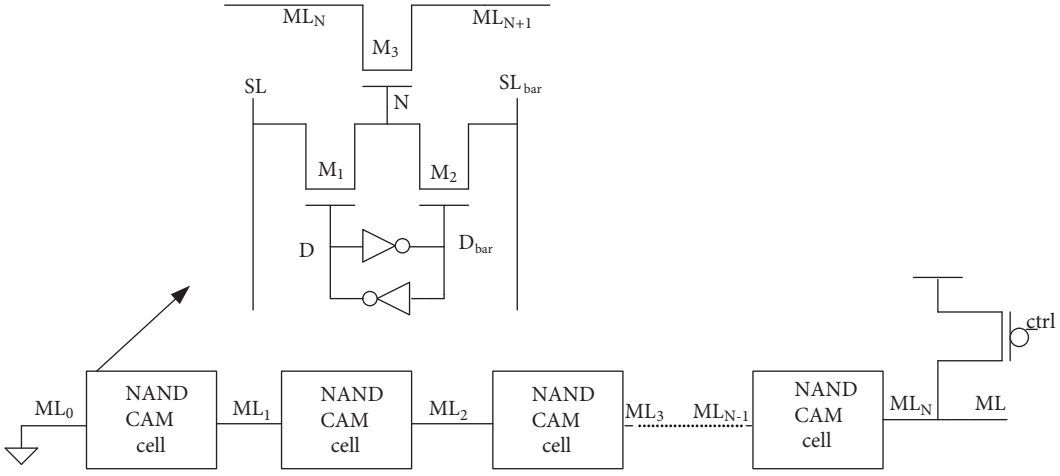

Figure 4. NAND CAM match-line architecture.

Table 2. Truth table for NAND CAM cell.

SL	D	ML	Output indicates
0	0	Match	Low
0	1	Miss	High
1	0	Miss	High
1	1	Match	Low

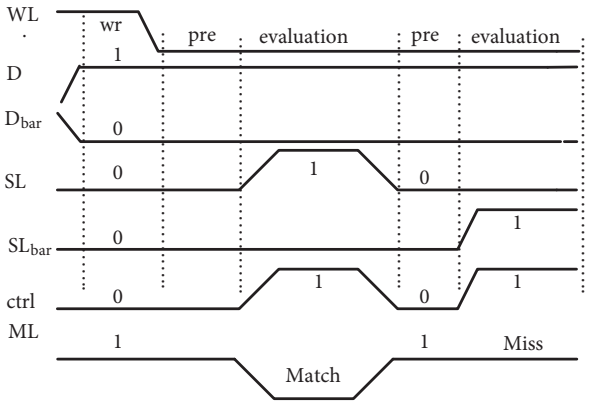

Figure 5. Timing waveform of NAND CAM cell for match followed by miss.

3. Short circuit current in NOR-type CAM

The power consumption of the NOR-type CAM design is possible in two phases: evaluation phase and precharge phase. It is identified that the power consumption of NOR CAM is high due to SC current path in the precharge phase during mismatch condition [16]. Consider a NOR CAM cell as shown in Figure 2. During the precharge phase, the *ctrl* signal is low and ML is precharged to V_{dd} through transistor P_1. In the evaluation phase, the output of ML depends on the search data input. Let us consider that the data stored in CAM cell is 1 such that $D = 1$ and $D_{bar} = 0$. If the input search word is also 1, match condition occurs and the ML is isolated from ground as M_1 and M_4 are in cutoff and no short circuit path exists from ML to the ground. However, if the search data input is 0 which is a mismatch condition, the transistors M_2 and M_4 are in saturation and they create a short circuit path from ML to ground. As ML drains from V_{dd} to ground, considerable amount of short circuit current will appear in the circuit. Similarly a short circuit path from ML to the ground through saturated M_1 and M_3 transistors will exist during the mismatch, with a stored 0 in the CAM cell.

3.1. Estimation of short circuit current for 4×3 NOR-type CAM

Consider a 4×3 NOR CAM with the given stored data as shown in Figure 6. During the precharge phase, all the four MLs (ML_1 to ML_4) charge to V_{dd}. Let us assume that, in the evaluation phase, a search word 101 is passed to the NOR CAM memory array. In this case, the second row matches with the input search word. Thus, the ML_2 is isolated from ground while other MLs have at least one mismatch condition marked with a dark line. Thus, the MLs drain from V_{dd} to ground and experience SC current. Table 3 shows the power consumption of NOR CAM cell during the precharge phase for a different match and mismatch conditions. The total contribution of power consumption during the match and mismatch is shown in a power chart in Figure 7. It is noted that the power consumption is high in the case of mismatch during the precharge phase due to SC current path, whereas in the case of a match, the power consumption is minimal and equal to that in the evaluation phase.

4. Precharge-free CAM architectures

All the works reported so far concentrated on switching power, whereas PF CAM and SCPF CAM concentrated on short circuit power. It is identified that precharging of ML consumes higher power due to short circuit current in NOR CAM. In [16], authors have proposed a pre-charge free CAM to reduce this short circuit current.

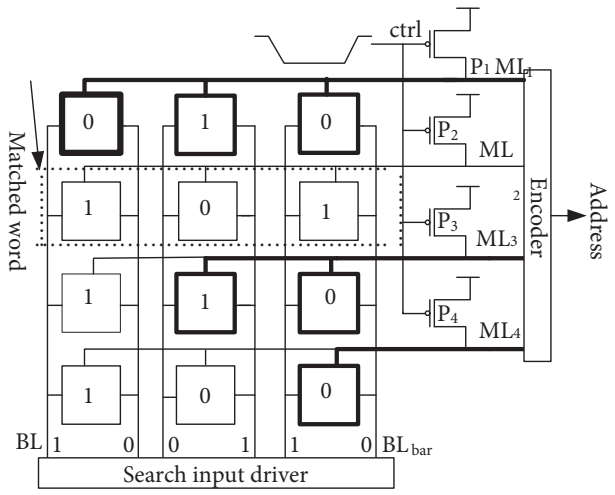

Figure 6. Estimation of SC current in 4×3 NOR-type CAM design.

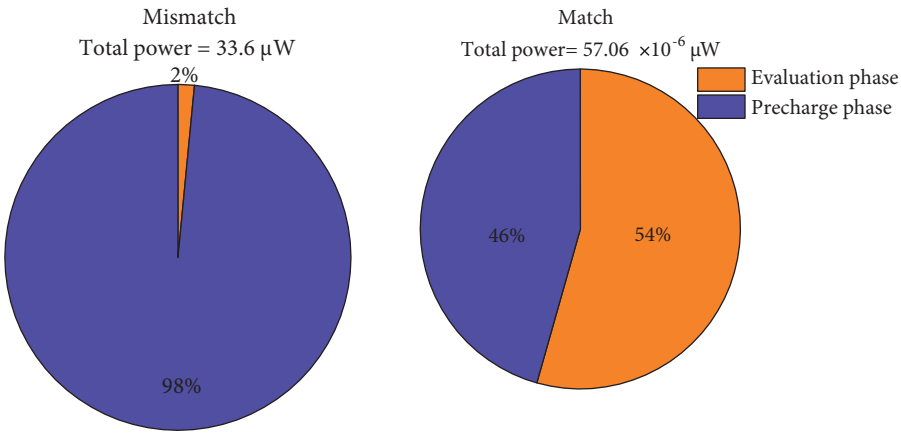

Figure 7. Power chart

Table 3. Power consumption of NOR-type CAM during the precharge phase.

Match-line	No. of CAM cells mismatching	No. of SC path	Power consumption in (μW)
ML_1	3	3	32.723
ML_2	0	0	26.03×10^{-6}
ML_3	2	2	25.128
ML_4	1	1	15.679

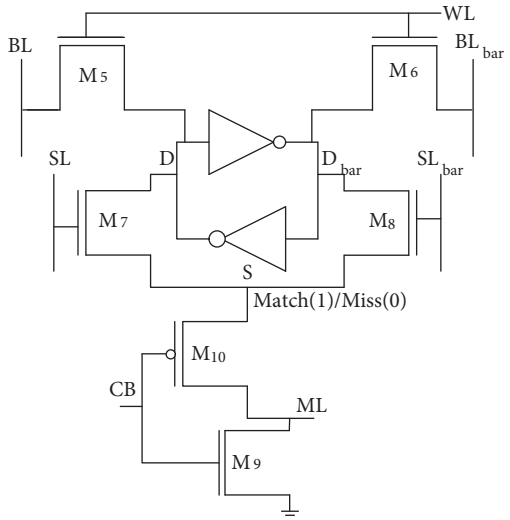

Figure 8. PF CAM cell

4.1. PF CAM

The circuit of PF CAM cell is shown in Figure 8. It consists of a 6T SRAM as a storage cell for writing the data. The NMOS transistors M_8 and M_7 are used as the comparison transistors. PMOS transistor M_{10} and NMOS transistor M_9 are used for controlling the ML output for match/miss based on control bit (CB) and charge value on node S. The purpose of CB is to reset the ML segments between two successive searches. This is accomplished by making CB high, which turns on pull-up transistor and drains ML irrespective of search

input word and stored word. Furthermore, during the search operation, CB =0, which makes M_{10} transistor ON and the pull-down transistor M_9 OFF. If there is a match, high charge value on node S makes ML charge through M_{10} transistor. In the case of a mismatch, low charge value on node S makes ML discharge through M_{10} transistor. PF CAM architecture formed by cascaded chain of control bits passing through CAM cell is shown in Figure 9. All the pull-up transistors M_{81}..... M_{8N} in the ML control circuitry are NMOSFETS except M_{80}. If a given input search word is matched with all the CAM cells in a specific row, then all the nodes S_1 to S_N will go high and drive transistors, M_{80} to M_{8N} into saturation. This makes the nodes ML_0 to ML_{N-1} to change and subsequently ML becoming high. Even if one CAM cell in a row mismatches, let us say third CAM cell, ML_2 discharges and M_{83} remains in cutoff and the ML discharges to low. It avoids short circuit path and charge-sharing problem and minimizes the overall power. However, due to the cascaded chain of control bits passing through CAM cells, the search operation is delayed significantly. To overcome this problem, SCPF CAM architecture is proposed.

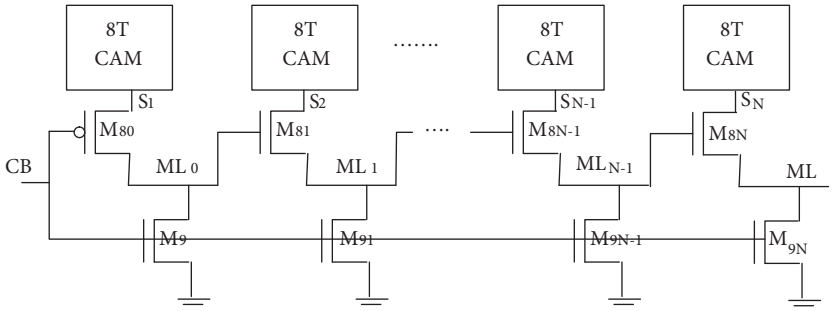

Figure 9. Match-line architecture for PF CAM.

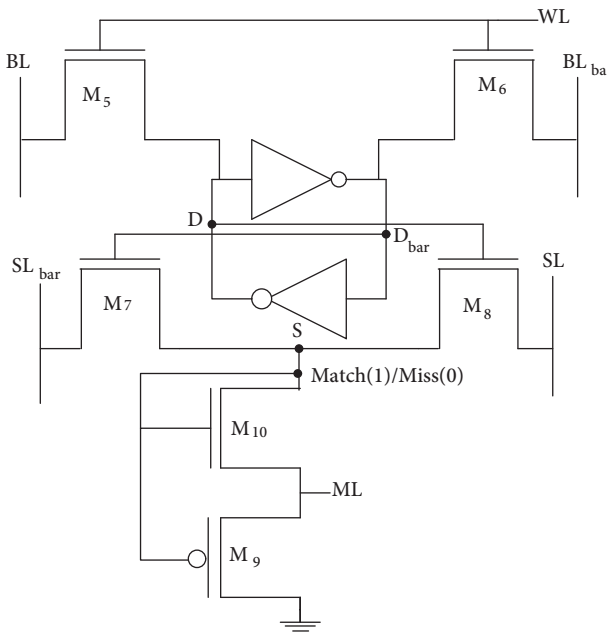

Figure 10. SCPF CAM cell.

4.2. SCPF CAM

The circuit of SCPF CAM cell is shown in Figure 10. It consists of a 6T SRAM cell, NMOS transistors M_{10}, M_7, M_8 along with a PMOS transistor M_9. The gates of M_8 and M_7 transistors are connected to complementary storage bits D and D_{bar}. When prestored data in a CAM cell is not matched with search input, charge value at node S is low and it is passed to ML through transistor M_9. In the case of a match, ML is driven by high voltage through transistor M_{10}. All the SCPF CAM cells are connected in parallel to form ML architecture as shown in Figure 11. Here, if all the prestored bits in a row are matched with input search word, charge value at all the mismatched nodes is high and ML attached to that row is also charged to high. When the prestored data in a row is not matched with input search word even by one bit, the charge value at all the nodes is low and the ML attached to that row will discharge to ground. By controlling the ML output with charges at the parallel nodes S_1, $S_2 ... S_N$, SCPF CAM ML structure overcomes the cascade ML structure of PF CAM and thus improves search speed significantly. However, SCPF CAM design utilizes one additional transistor per CAM cell, when compared to PF CAM architecture which is responsible for an increase in power as well as cell area. We propose a hybrid self controlled precharge-free (HSCPF) CAM architecture, which overcomes the search delay problem of PF CAM and power consumption problem of SCPF CAM.

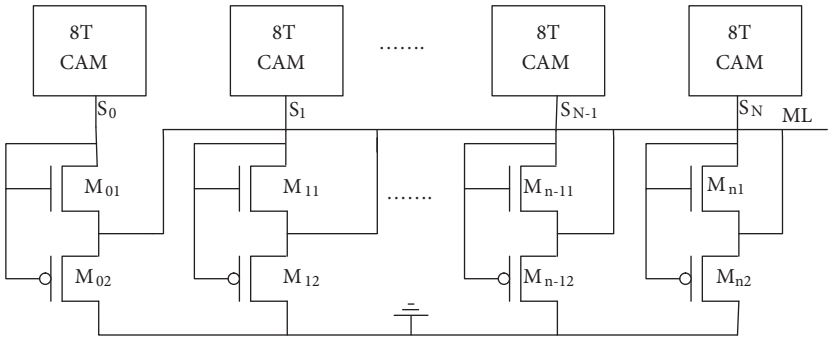

Figure 11. Match-line architecture for SCPF CAM.

5. Proposed HSCPF CAM

The architecture of the proposed HSCPF CAM cell consists of a two 6T SRAM cells, with four NMOS transistors M_7, M_8, M_{17}, and M_{18}. We use a hybrid charge control circuitry, which controls two consecutive CAM cells. It consists of M_9 and M_{10} transistors as shown in Figure 12. The gates of M_9 and M_{10} transistors are connected to node S_1 and the source of M_{10} transistor is connected to node S_0.

- In this charge control circuit, charge values at nodes S_0 and S_1 control the ML output for high or low. If the prestored data in two CAM cells is matched with the search input, the charge value at nodes S_0 and S_1 is high which in turn passes a high value to ML through transistors M_9 and M_{10}, else it passes low value. These two CAM cells will be considered a CAM word for further operation.
- All these CAM words are connected in parallel to constitute ML structure as shown in Figure 13. If the search content matches with the prestored data in the first CAM word, the charge values at the nodes S_0 and S_1 are high. This process continues for the remaining CAM words in the ML structure until nodes S_{N-1} and S_N. If all the prestored bits in a word are matched with the input search word, the ML attached to that word charges to high. In the case where prestored bits in a word are not matched with the input search word even by one bit, the ML attached to that word charges to low.

Table 4 shows the truth table of HSCPF CAM cell for match/miss. The representation of timing waveform of HSCPF CAM designs is shown in Figure 14.

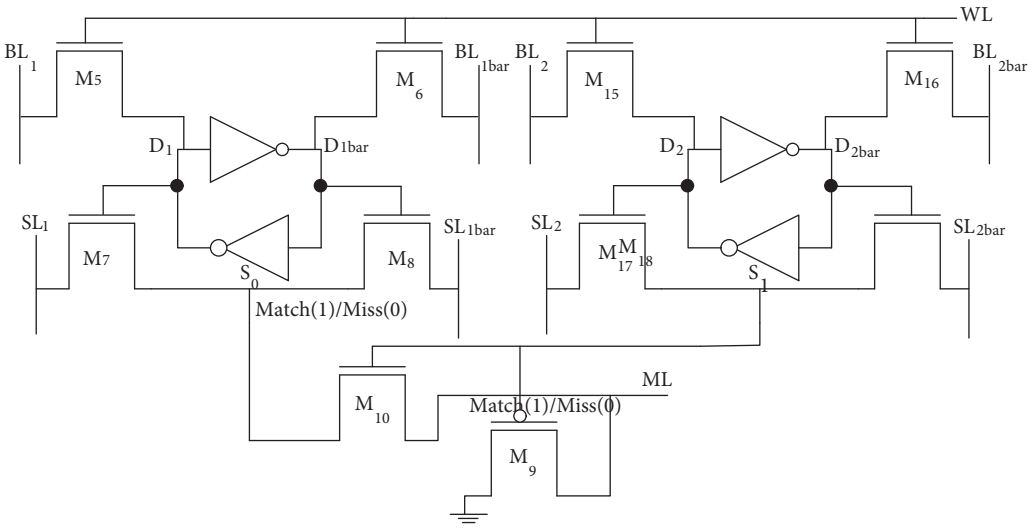

Figure 12. HSCPF CAM cell.

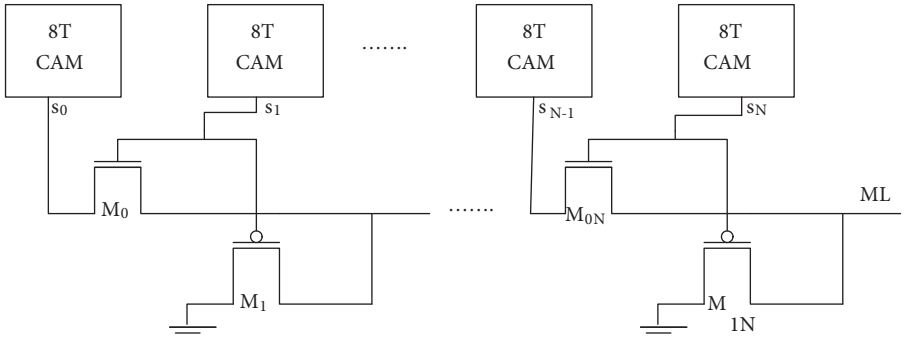

Figure 13. Match-line architecture for HSCPF CAM.

Total time required to complete one clock cycle for HSCPF CAM ML architecture is given by Eq. (7)

$$T_{totprefree} = T_{wr} + T_{SL}, \tag{7}$$

where t_{wr} = write time and t_{SL} = evaluation time or search time.

It can be observed from the architecture that HSCPF CAM utilizes two transistors per a two-bit word for the charge control circuitry; hence, the number of transistors utilized for the charge control circuitry is half of that used in SCPF CAM. Therefore, the HSCPF CAM minimizes the area as well as power consumption. The proposed HSCPF CAM overcomes the cascaded ML structure of PF CAM and increased transistor count of SCPF CAM, thereby offering lower energy metric when compared to SCPF CAM and PF CAM.

6. Simulation results

The proposed HSCPF CAM design of size 8 (words) × 8 (bits) is implemented in the technology node 45-nm using generic process design kit(GPDK) and simulations are performed for validation using Virtuoso tool.

Table 4. Truth table of HSCPF CAM cell.

S0	S1	ML	Output indicates
0	0	Miss	Low
0	1	Miss	Low
1	0	Miss	Low
1	1	Match	High

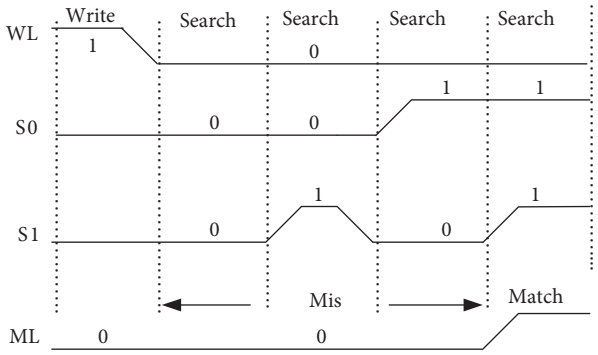

Figure 14. Timing waveform of HSCPF CAM.

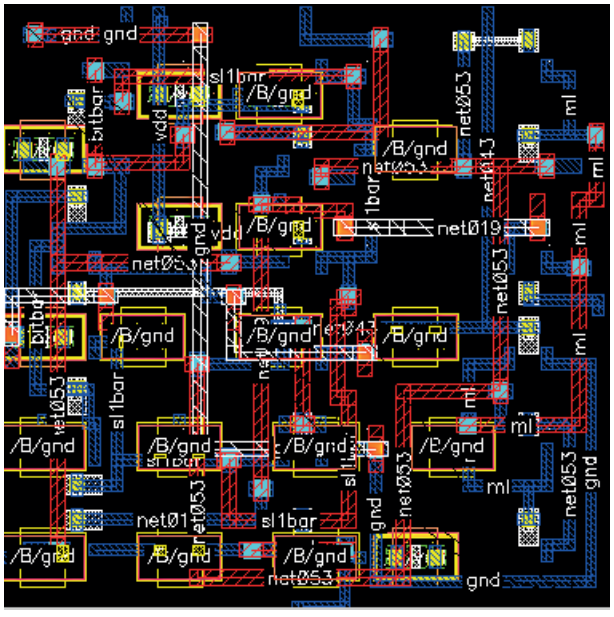

Figure 15. Partial layout of the proposed CAM.

Along with the proposed design, basic NAND- and NOR-type ML CAMs, precharge-free CAMs of [16] and [17] of size 8 × 8 are also simulated. These designs are compared with the proposed design for power, search delay, and energy-metric. Partial layout view of the proposed CAM cell design is shown in Figure 15. This is verified in Cadence Virtuoso for DRC and LVS check. The area of HSCPF CAM design is smaller than those of other conventional CAM designs because the charge control circuitry is shared between two successive CAM cells and also the proposed design uses folding and chaining of transistor in CAM structure during layout

design. A 500 run of Monte Carlo (MC) simulations is performed with 3 σ Gaussian distribution by varying the design parameters, process corners, and operating temperature. Figures 16 and 17 show the simulations of performance metric average across 500 MC runs. The search delay and power consumption are 127.28 (pS) and 0.273 (mW), respectively. Table 5 presents the comparison summary of the proposed and previous CAM designs. The results show that the proposed design exhibits a power reduction of 3.181% over PF CAM and 18.39% over SCPF CAM. In the case of search delay, proposed HSCPF CAM design shows 73.87% reduction over PF CAM and 26.73% reduction over SCPF CAM. HSCPF CAM design shows 96.90% reduction over NOR CAM, 88.96% reduction over NAND CAM, 74.71% reduction over PF CAM and 40.14% reduction over SCPF CAM in energy metric.

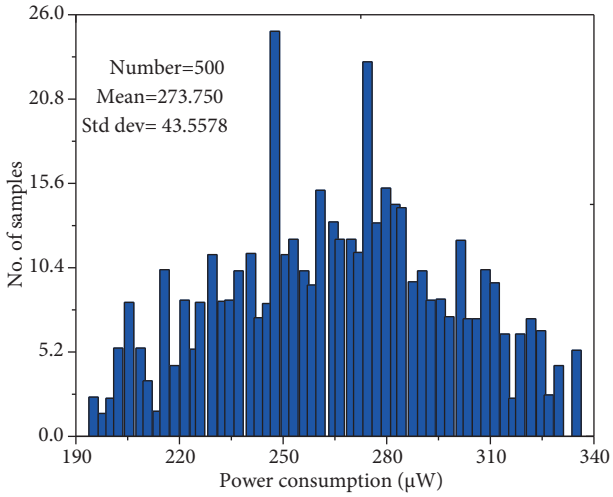

Figure 16. Histogram of power consumption.

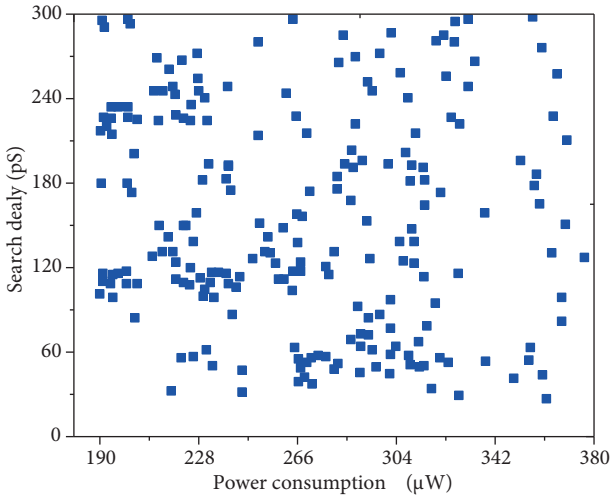

Figure 17. Scattered plot of search delay against power consumption.

To estimate the contribution of SC power to the total power, simulations are performed on conventional NOR CAM and proposed HSCPF CAM designs. The match case and mismatch case power consumption of conventional NOR CAM are 0.293 mW and 1.932 mW, respectively and those of HSCPF CAM are 0.207 mW and 0.218 mW, respectively. From these results, we can observe that the conventional NOR CAM consumes more power during mismatch case because of SC. As SC is eliminated in the proposed HSCPF CAM, the power consumed by it during mismatch case is much smaller when compared to the conventional NOR CAM. Hence, we can claim that the proposed design saves 86.98% of total power which is attributed by SC power.

Different process corner simulations like SS (slow NMOS and slow PMOS), FF (fast NMOS and fast PMOS), FS (fast NMOS and slow PMOS), and SF (slow PMOS and fast NMOS) for worst case match followed by miss are evaluated. The best case search delay and power of the proposed design are 29.4 (pS) and 0.168 (mW), respectively, and its worst case search delay and power are 302 (pS) and 0.792 (mW), respectively. Figures 18 and 19 show process corner simulations for search delay and energy metric. The results show that the power consumption and search delay average over process corners is 0.273 (mW) and 133.48 (pS). To validate a CAM design, the simulations are performed on the proposed design for higher order bit length up to 128 bits. Even for a longer word length, the proposed design functions properly during miss/match case. The simulations performed by varying different lengths for power consumption and energy metric are shown in Table 6. As the size of the CAM array increases, there is gradual increment in power consumption. However, the energy metric

is maintained almost constant for the CAM arrays of different sizes and hence it is evident from the results that the proposed design is efficient in terms of area and energy-metric. Therefore, this design is suitable for constructing CAM with low power and high-speed applications for longer word lengths.

Table 5. Comparison summary with previous works.

Type of 8×8 CAM	NOR	NAND	PF	SCPF	HSCPF
Ref	Conventional	Conventional	[16]	[17]	Proposed
Search delay (pS)	265.2	808	283.2	101	74
Power consumption (mW)	1.92	0.177	0.22	0.261	0.213
Energy metric (fJ/bit/search)	7.956	2.23	0.973	0.411	0.246
Area (μm^2)	792.12	777.74	768.28	797.64	738.12

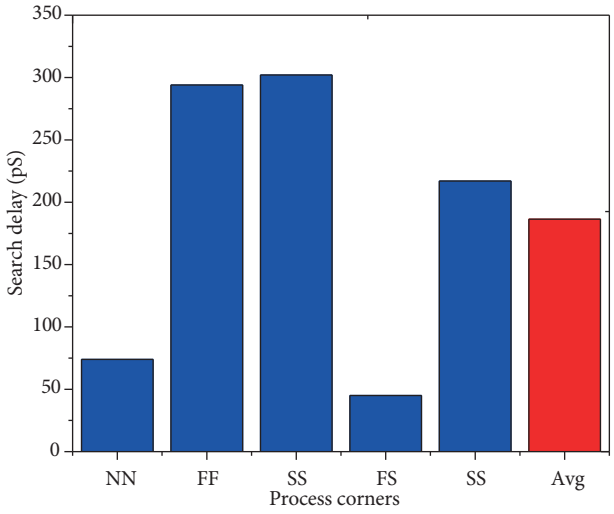

Figure 18. Search delay at process corners.

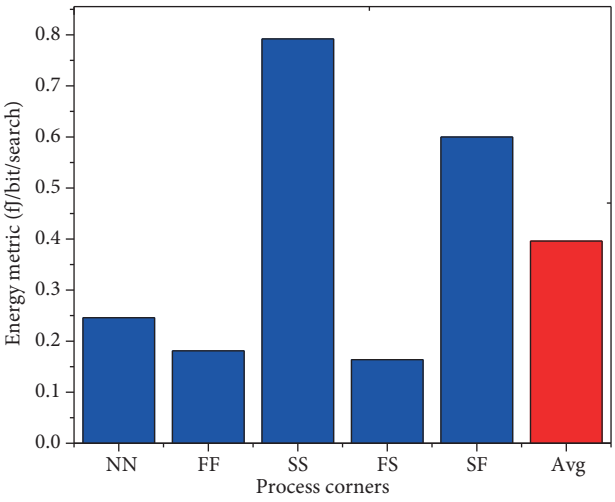

Figure 19. Energy metric versus process corners.

7. Conclusion

In this paper a low energy-metric HSCPF CAM design has been presented. The proposed design features a new charge control circuitry which can be shared between two successive CAM cells, thereby considerably reducing the number of transistors required for charge control circuitry. The proposed ML architecture is simulated for different process corners and MC simulations at 45nm technology node CMOS process with 1 V supply voltage. The proposed design significantly reduces the search delay, power, as well as energy metric when compared to PF CAM and SCPF CAM as it has charge control circuitry with less number of transistors than SCPF CAM

Table 6. Power and energy metric dependency of ML bit length of single word for the proposed design.

ML section length	P_{avg} (μW)	Energy metric (fJ/bit/search)
8 bit	26.71	0246
16bit	53.42	0.248
32bit	106.85	0.254
64bit	213.71	0.257
128bit	427.42	0.259

and avoids the cascaded ML architecture of PF CAM. The results show that the proposed HSCPF CAM is best suited for low energy metric high-speed table lookup.

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