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Characterization of a high-speed radio-frequency sampling and demultiplexing circuit based on the cascade connection of pin photodiodes

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Abstract: Herein, we apply theoretical models to characterize the transfer function and frequency response of a complex optoelectronic circuit that comprises a primary ultrafast sampling circuit followed by a cascade connection of N demultiplexing stages. The successive radio-frequency optoelectronic samplers were based on the cascade connection of positive-intrinsic-negative-photodiodes (PIN-PDs). We developed a procedure to calculate the principal design parameters that allows us to use optical power for each sampling and demultiplexing stage, such that the circuit can be designed based on the application requirements. The results obtained from the theoretical models were compared with the measurements obtained from the 2.5 GS/s sampling circuit connected in cascade with a 1.25 GS/s and a 625 MS/s demultiplexing circuit implemented using commercial PIN-PDs.

Key words: Optoelectronics sampling circuit, PIN photodiode, radio-frequency sampled signal, frequency response

1. Introduction

An optoelectronic switch implemented with a positive-intrinsic-negative-photodiode (PIN-PD) uses the resistance dependence of the optical power impinging on the PIN-PD to implement the switching function. The PIN-PD resistance value can be varied from approximately 100 kΩ to less than 1 Ω for a milliwatt change in the optical power across it. A majority of photodiodes exhibit this characteristic, but the PIN-PD is optimized to achieve a relatively wide resistance range, good linearity, low distortion, and low current drive [1]. The characteristics of the PIN-PD make it suitable for use in switches [2], modulators [3], phase shifters [4], signal mixers [5], sensors [6], and other signal-control circuits [7]. Switching applications of PIN-PDs, such as antenna-array switching and optically triggered sampling circuits for photonics analog-to-digital converters, are important when optically triggered switches are used for multigigabit-per-second radio-frequency (RF) sampling [8, 9]. Electro-optic modulators have been widely employed in optical sampling schemes to convert and digitize electrical analog signal amplitudes into corresponding optical bit streams. In these optical sampling schemes, electrical-to-optical transducers are needed to reconvert optical samples into electrical signals so that the quantization functions can be performed using an electronic circuitry. Also, if the sampled data rate exceeds the available processing speed of a single electronic quantizer, intermediate demultiplexing stages are required to demultiplex different phases of the sampled signal to yield a quantizer's arrangement of low multichannel data rates. In this type of sampling scheme, the optical-to-electrical and electrical-to-optical transducers create

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bottlenecks that diminish the sampling process quality [10–13]. Similarly, the demultiplexers create bottlenecks that limit the sampling rate.

In the last few years, sampling and demultiplexing architectures based on PIN-PDs have been reported as improvements on the sampling schemes based on electro-optic modulators [14, 15]. A unique feature of this sampling and demultiplexing architecture is that the electrical-in to electrical-out signal transfer is maintained for the optoelectronic sampling and demultiplexing circuits. In addition, clocks for the activation of the sampling and demultiplexing circuits are generated from a single-laser source using passive optical components. The use of passive optical components does not introduce extra jitter, which reduces the timing-error effects and eliminates the need for external synchronization signals for improving the system performance [15].

To characterize the performance of the optoelectronic sampling and demultiplexing circuits, it is necessary to determine the voltage attenuation of the RF-sampled signal when this signal propagates through the cascaded stages because of the voltage dividers given by the equivalent-resistive circuits. Also, the complete circuit bandwidth and the individual stage bandwidth will be limited by the intrinsic capacitances of the PIN-PDs and the load resistors. In this paper, we develop a procedure to calculate the principal design parameters. The procedure allows us to use the optical powers applied to each PIN-PD to design the sampling and demultiplexing circuit according to the application requirements. In addition, the results obtained from the theoretical models are compared with the measurements obtained from the 2.5 GS/s sampling circuit connected in cascade with a 1.25 GS/s circuit and a 625 MS/s demultiplexing circuit implemented using commercial PIN-PDs.

2. Optoelectronics sampling and demultiplexing circuit

Figure 1 shows the basic optoelectronic sampling circuit. The RF input signal (to be sampled) is connected in series with a reverse-biased PIN-PD and a load resistor. The PIN-PD in the circuit acts as a fast normally off optoelectronic switch whose *ON/OFF* states are actuated by optical pulses. In its *OFF* state, i.e. in the absence of an optical trigger, the PIN-PD maintains high impedance causing an open current path in the series circuit arrangement with no voltage developed across the load resistor. However, in its *ON* state, that is, when a laser pulse impinges on the PIN-PD, its impedance is low; this allows the current through the circuit and results in a voltage across the load resistor. Thus, when a stream of laser pulses at the repetition rate f impinges upon the PIN-PD, the amplitude of the input RF signal will accordingly be sampled at the same rate, and the sampled data will appear across the load [16].

Figure 2 shows a cascade connection of the sampling circuit with two demultiplexing stages. D1 in the sampler circuit is activated by a primary optical signal (f) resulting in sampled RF data across the load resistor (R1). The output of the sampling circuit is split into two channels and fed to the inputs of two demultiplexers designated as even and odd demultiplexing stages. The photodiodes in the odd and even demultiplexing stages (D2 and D4) are activated by their corresponding optical signals f_o and f_e, whose optical pulses line up with the odd and even optical pulses, respectively, of the primary optical signal f; here, the repetition frequencies f_o and f_e are the submultiples of the primary frequency. When the optical pulses of f_o and f_e impinge upon D2 and D4, the odd and even samples from the main sampled RF signal are demultiplexed to form a pair of new discrete time signals y1[n] and y2[n]. For simplicity, in the second demultiplexing stage, the circuit shows only the PIN-PDs (D3 and D4) that demultiplex the odd samples (odd/odd) and the even samples (even/odd) of the original odd demultiplexed signal. Hence, the output of the odd demultiplexer circuit is split into two channels and fed to the inputs of the odd/odd and even/odd demultiplexing stages. The photodiodes in the

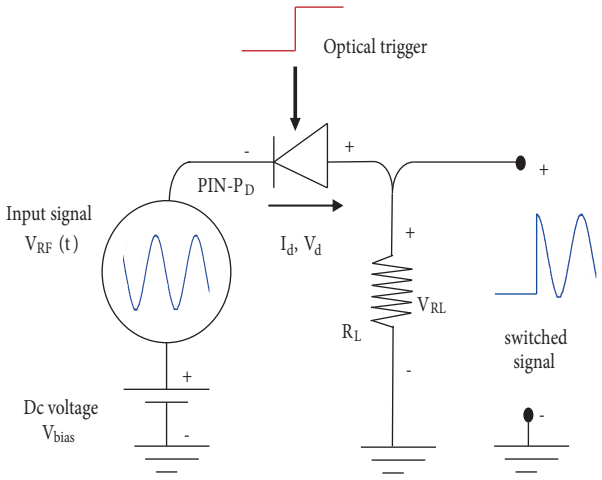

Figure 1. Basic PIN-PD-based sampling circuit.

odd/odd and even/odd demultiplexers (D3 and D5) are activated by the optical signals f_{oo} and f_{ee}, whose optical pulses line up with the odd/odd and even/odd optical pulses, respectively, of the secondary optical signal f_o. Here also, the repetition frequencies of f_{oo} and f_{ee} are respectively submultiples of f_o and f_e. When the optical pulses of f_{oo} and f_{ee} impinge upon D3 and D5, the odd/odd and even/odd sampled data bit streams from the odd RF samples are demultiplexed to form a pair of new discrete time signals y3[n] and y4[n] [14, 16, 17].

3. Analysis and modeling

In the optoelectronics sampling circuit of Figure 1, the DC reverse-bias voltage enables the photodiode to work in an operation point in which the electric current across it depends on the applied optical power P. Hence, the switching function is controlled by applying P in the PIN-PD. For the indium gallium arsenide (InGaAs) PIN-PD listed in the Table, Figure 3 shows the real I−V curve measurement for an applied P of 0 mW, 2 mW, 3 mW, and 6 mW. This PIN-PD has a reverse saturation current $I_{sat} = 0.2$ nA and responsivity $\Re$ was 0.95 A/W at a wavelength of 1550 nm. To ensure a range of linear excursions for the peak-to-peak voltage input signal $V_{RF}(t)$, an operation point for the PIN-PD can be strategically selected [18–20]. For example, Figure 3 shows the position of an operation point at $V_d = 0.710$ V and $I_d = 2.18$ mA on the $P = 6$ mW curve. For the shown operation point, $k = 23.4977$ is calculated from $I_d = -I_{sat}(e^{kV_d}-1) + I_{ph}$, where $I_{ph} = P\Re$ is the photogenerated current. The ideality factor $n = 1.6463$ is calculated using $n = q/k_BTk$ where q is the electron charge, k_B is the Boltzmann constant, and T is temperature in Kelvin. In addition, a photodiode small-signal resistance $R_d = 2.09\ \Omega$ was calculated using (1) [18].

$$R_d = \frac{1}{kI_{sat}e^{kV_d}} \tag{1}$$

In the presence of an optical pulse, the voltage drop across the load resistor depends on the amplitude of the RF analog input signal (in the optical pulse impinging instant t), the ratio of the load resistance, and the PIN-PD small-signal resistance $V_{RL} = V_{RF}(t)R_L/(R_L + R_d)$. The sampled signal (i.e. the voltage in the load V_{RL}) suffers an attenuation A relative to the input signal V_{RF} given by $A = (V_{RF} - V_{RL})/V_{RF}$.

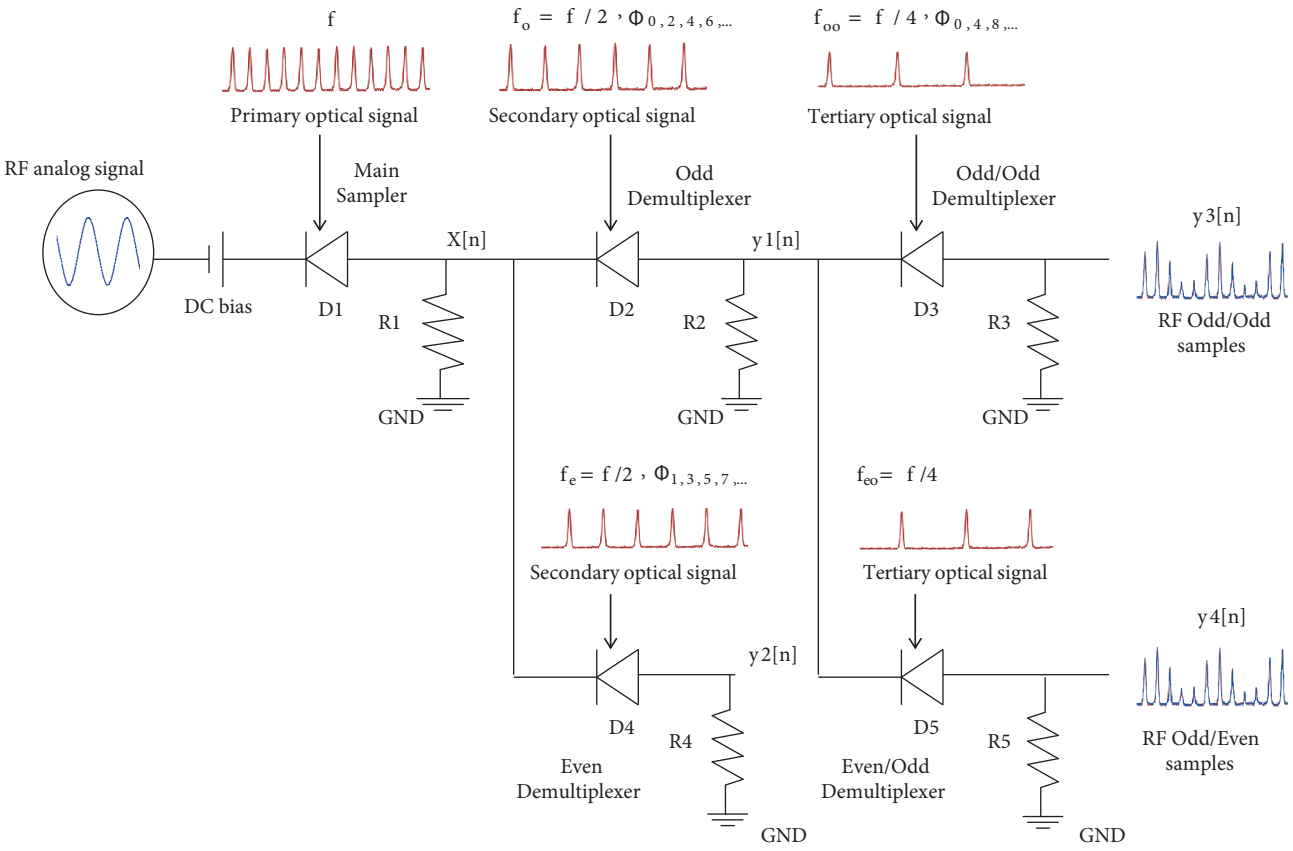

Figure 2. Schematic circuit of the optoelectronic sampling and demultiplexing circuit.

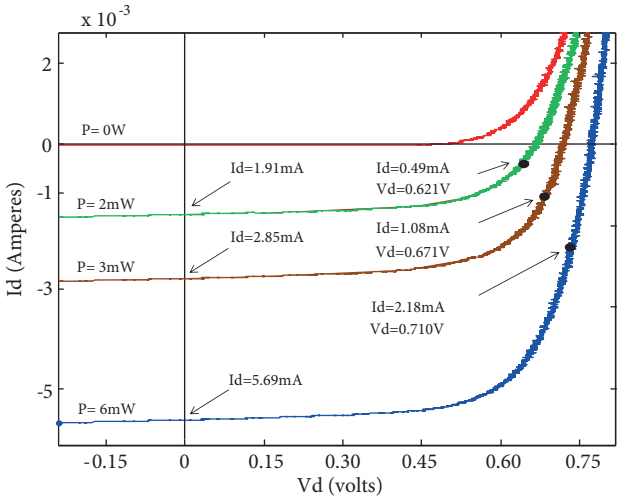

Figure 3. Measured I−V curve of an optically triggered switch based on an InGaAs PIN-PD, with $I_{sat} = 20$ nA, $R = 0.95$ A/W at $\lambda = 1550$ nm, and different optical peak power.

By relating these two equations, the attenuation A is given by $A = R_d/(R_L + R_d)$. In the circuit shown in Figure 2, the most critical case because of impedance matching is given when the optical signals simultaneously activate all stages. The attenuation will increase as the RF-sampled signal propagates through the sampling and demultiplexing stages. The load resistance of the first stage R_{L1} is modified by the parallel connection

Table. Relevant devices' characteristics.

Device	**Model**	**Specification**
Laser source Onefive	Genki-15	Pulse width > 5 ps Aver. output $= 150$ mW $\lambda = 1550$ nm
InGaAs PIN Photodiode AC photonics	PTD2212−HL	Cutoff freq. $= 3$ GHz Responsivity $= 0.95$ A/W $I_{sat} = 0.2$ nA
1×2 optical splitter SQS	70/30 PLC asymmetrical splitter	Splitting ratio $= 70/30$ Max. insertion loss $= 3$ dB $\lambda = 1260 - 1650$ nm
Manual variable optical attenuator Thorlabs	VOA50−FC	Atten. range $= 1.5$–50 dB Atten. resolution $= 0.1$ dB $\lambda = 1200 - 1600$ nm
Manual variable optical delay line SAMTEC	ODL340−S−09 − 10	$\lambda = 1510 - 1650$ nm Delay range $= 0$–330 ps Insertion loss $= \pm 1$ dB

with the resistors of the subsequent stages, which results in an equivalent resistance R_{LT1}. Similary, the load resistance of the ith stage is modified by the subsequent stage to give $R_{LTi} = R_{Li}//(R_{d(i+1)} + R_{LT(i+1)})$.

For the first stage, the equivalent resistance and the optical power applied to the PIN-PDs are related by $A_1 = R_{d1}/(R_{LT1} + R_{d1})$. Solving for R_{LT1}, we have $R_{LT1} = (R_{d1}/A_1) - R_{d1}$. R_{d1} is optical-power-dependent; therefore, R_{LT1} is also optical-power-dependent. Hence, for the ith stage, we have:

$$R_{LTi} = \frac{R_{di}}{A_i} - R_{di} \tag{2}$$

The attenuation of the RF signal in stage i must be greater than the attenuation in stage $i-1$ because the attenuation increases in the subsequent stage. For the last stage, load resistor $R_{LTn} = R_{Ln}$; however, for the previous stages, the parallel resistance with the adjacent stages must be taken into account, which results in:

$$R_{LTi} = \frac{R_{Li}(R_{d(i+1)} + R_{LT(i+1)})}{R_{Li} + (R_{d(i+1)} + R_{LT(i+1)})} \tag{3}$$

R_{di} can be calculated by using Eq. (1) for a desired attenuation A_i; therefore, an equivalent resistor R_{LTi} can be obtained using Eq. (2). Furthermore, this R_{LTi} value can be used in Eq. (3) to solve R_L, obtaining:

$$R_{Li} = \frac{(R_{d(i+1)} + R_{LT(i+1)})(R_{di}/A_i - R_{di})}{(R_{d(i+1)} + R_{LT(i+1)}) - (R_{di}/A_i - R_{di})} \tag{4}$$

To obtain a positive value of R_{Li} in Eq. (4) the inequality $(R_{d(i+1)} + R_{LT(i+1)}) > (R_{di}/A_i – R_{di})$ must be satisfied. Then, the restriction $P_i > P_{i+1}$ is imposed because, in Eq. (1), R_d is inversely proportional to the applied optical power P_i.

3.1. Sampling circuit transfer function

To analyze the dynamic response of the sampling circuit, we considered C_i, the internal capacitance of the PIN-PDs, because this parameter limits the response speed. Therefore, the circuit shown in Figure 2 is represented by the diagram in Figure 4. The differential equations describing the behavior of the sampling circuit are:

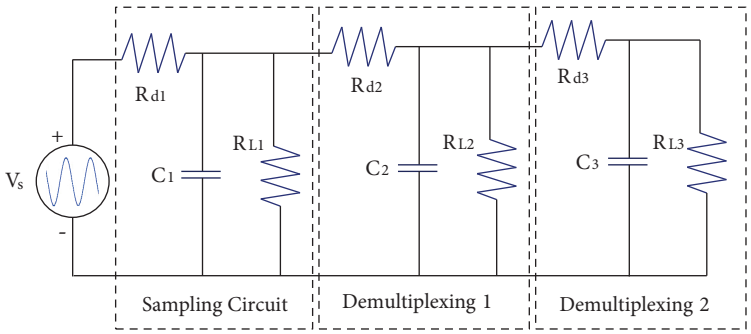

Figure 4. Circuit to compute the transfer function of the sampling circuit in cascade connection with two demultiplexing stages.

$$i(t) = i_{C_1}(t) + i_{RL1}(t)$$

Where:

$$i(t) = C_1 \frac{d}{dt} V_c(t) + V_{RL1}(t)/R_{LT1} \tag{5}$$

$$i(t) = \left[V_s(t) - V_{RLT1}(t)\right]/R_{d1} \tag{6}$$

Equating the Laplace transform of Eqs. (5) and (6), the transfer function (output/input relationship) of the sampling circuit is given by Eq. (7), where $V_s(s)$ is the input signal and $V_{RL1}(s)$ is the output signal.

$$FT_1 = \frac{V_{RL1}(s)}{V_s(s)} = \frac{R_{LT1}}{R_{d1} + R_{LT1}} \left(\frac{1/T_1}{s + 1/T_1} \right) \tag{7}$$

FT_1 represents a first-order system, and $T_1 = R_{LT1} R_{d1} C_1/(R_{d1} + R_{LT1})$ is the constant of the time of a circuit. Three differential equations can be obtained from a nodal analysis for $V_{RL1}(t)$, $V_{RL2}(t)$, and $V_{RL3}(t)$ of the overall circuit in Figure 4. The Laplace transforms of these equations are given by:

$$V_s(s) = V_{RL1}(s) \left[R_{d1} C_1 + 1 + \frac{R_{d1}}{R_{L1}} + \frac{R_{d1}}{R_{L2}} \right] - V_{RL2}(s) \frac{R_{d1}}{R_{d2}} \tag{8}$$

$$0 = -V_{RL1}(s) + V_{RL2}(s) \left[R_{d2} C_2 s + 1 + \frac{R_{d2}}{R_{L2}} + \frac{R_{d2}}{R_{L3}} \right] - V_{RL3}(s) \frac{R_{d2}}{R_{d3}} \tag{9}$$

$$0 = -V_{RL2}(s) + V_{RL3}(s) \left[R_{d3} C_3 s + 1 + \frac{R_{d3}}{R_{L3}} \right] \tag{10}$$

Eqs. (8), (9), and (10) can be represented in matrix form as:

$$\begin{bmatrix} R_{d1}C_1 + 1 + \frac{R_{d1}}{R_{L1}} + \frac{R_{d1}}{R_{L2}}, & -\frac{R_{d1}}{R_{d2}}, & 0 \\ -1 & R_{d2}C_2 s + 1 + \frac{R_{d2}}{R_{L2}} + \frac{R_{d2}}{R_{L3}}, & -\frac{R_{d2}}{R_{d3}} \\ 0, & -1, & R_{d3}C_3 s + 1 + \frac{R_{d3}}{R_{L3}} \end{bmatrix} \begin{bmatrix} V_{RL1}(s) \\ V_{RL2}(s) \\ V_{RL3}(s) \end{bmatrix} = \begin{bmatrix} V_s(s) \\ 0 \\ 0 \end{bmatrix} \tag{11}$$

From the system of equations given by Eq. (11), the transfer function of the overall circuit is calculated as $V_{RL3}(s)/V_s(s)$. The partial transfer functions $V_{RL2}/V_s(s)$ and $V_{RL1}/V_s(s)$ can also be obtained. For a large

circuit (more demultiplexing stages), the system can be solved by expanding it into more equations (i.e. more nodes) to find the overall transfer function; the square matrix is composed of the system's parameters.

3.2. Frequency response

To obtain the cutoff frequency of the sampling circuit, the absolute value of the transfer function was computed by replacing the Laplace variable s by the complex angular frequency $j\omega = s$ [21]. Furthermore, this value was equated with the gain factor $|FT_1(j\omega)| = K_1/\sqrt{2}$ and solved for ω. Hence, from Eq. (7), we have the sampling circuit:

$$|FT_1(j\omega)| = \left|\left(\frac{K_1}{1+jT_1\omega}\right)\right| = \frac{K_1}{\sqrt{1+T_1^2\omega^2}} = \frac{K_1}{\sqrt{2}} \tag{12}$$

Here, $K_1 = R_{LT1}/(R_{d1}+R_{LT1})$ is the peak gain. Solving for the angular frequency, we obtain $\omega_c = 1/T_1$. For the overall circuit, the same procedure is applied to the transfer function obtained in the previous section.

4. Implementation and results

To test the functionality of the previously developed equations, we designed and implemented a sampling circuit in the cascade connection with two demultiplexing stages (see Figure 5). The Table lists the device characteristics used in the implementation. A 40 MHz sinusoidal signal with a 300 mV peak amplitude was used as the RF input signal. The primary optical clock pulses were obtained from a 625 MHz, 150 mW pulsed laser source Genki-15. Passive optical components were cascaded to generate clock signals from the laser source with optical pulses repetition rates of 2.5 GHz, 1.25 GHz, and 625 MHz. Manual variable optical delay lines and a single-mode optical fiber were used to implement the passive delay lines.

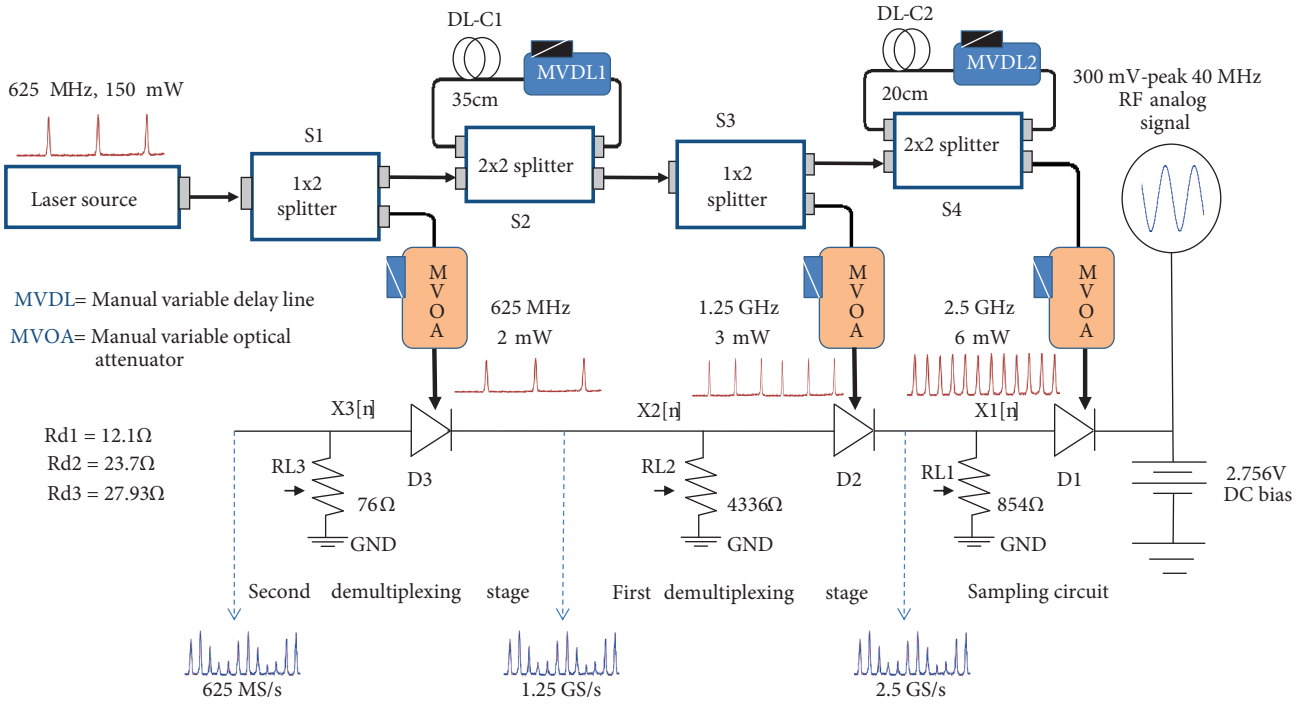

Figure 5. Schematic circuit of the experimental set-up.

In the circuit shown in Figure 5, the main 625 MHz optical signal forming the laser source is split into two using the 70/30 asymmetrical splitter S1. The signal emerging from the lower output port of S1 was properly attenuated by a manual variable optical attenuator (MVOA) and then used to activate the PIN-PD (D3) in the second demultiplexing stage. Simultaneously, the signal emerging from the upper output port of S1 was fed into the lower input port of a frequency-doubling optical circuit composed of the 2×2 coupler S2. The upper output port of S2 was fed back into its upper input port by using a series connection of a loop of optical fibers 35 cm long and $MVDL1$. Proper tuning of $MVDL1$ doubles the input frequency from 625 MHz to 1.25 GHz at the output of S2. Furthermore, the optical signal forming the lower port of S2 is split into two using the 70/30 asymmetrical splitter S3. The signal emerging from the lower output port of S3 is properly attenuated by an MVOA and then used to activate the PIN-PD (D2) in the first demultiplexing stage. The signal emerging from the upper output port of S3 is fed into the lower input port of a frequency-doubling optical circuit composed of the 2×2 optical coupler S4. The upper output port of S4 was fed back into its upper input port by using a series connection of a loop of optical fiber that was 20 cm long and $MVDL2$. Proper tuning of $MVDL2$ doubles the input frequency from 1.25 GHz to 2.5 GHz at the output of S4. The signal emerging from the lower output port of S4 is properly attenuated by an MVOA and then used to activate the PIN-PD (D1) in the sampling circuit.

In addition, Figure 5 shows the calculated load resistance R_L and the small-resistance R_d for the desired attenuations of 10%, 19%, and 27% in the sampling circuit, the first and the second demultiplexing stages, respectively. The values of R_L and R_d were obtained using Eqs. (1) and (4) following the procedure given in the Appendix. From Figure 5, we see that the observed load resistances are in the range between tens of ohms and thousands of ohms; these are typical resistance values. However, the small-signal resistance values are less than 100 Ω, which is consistent with the theory explained previously. Figure 6 shows the plots that compare the measurements with the calculated curves obtained from the transfer function equation derived in Section 3. Figure 6a shows the outputs of the 2.5 GSPS sampling circuit, and Figures 6b and 6c show the outputs of the 1.25 GSPS and 625 MSPS demultiplexing circuits, respectively. The measurements were made using the HP Digital Communication Analyzer 83480A. The measured attenuations shown in Figure 6 are consistent with the theoretical values used in the calculations.

Figure 7 shows a comparison between the theoretical and real measurements of the frequency response of the circuit. For calculations, we used a capacitance of $C_i = 0.75$ pF for the PIN-PDs. The theoretical curve was obtained by plotting a Bode diagram from the transfer function of the sampling and demultiplexing circuit obtained by using Eq. (11). The measured curve was obtained by using the S-parameter network analyzer 8753ES from Agilent. By comparison, we observed that the measurements and the theoretical results matched well at the cutoff frequency calculation obtained from Eq. (12). In addition, we observed that the RF-sampled signal at the output of the second demultiplexing stage has an attenuation of approximately 27% (i.e. 0.72 of the magnitude) and it had a magnitude of 0.509 ($\approx 0.72/\sqrt{2}$) at the cutoff frequency Fc of 2.52 GHz; these values are consistent with the desired theoretical values.

5. Conclusions

In this study, we developed a straightforward procedure that uses theoretical models to characterize the transfer function and the frequency response of a complex optoelectronic circuit comprising a primary ultrafast sampling circuit followed by cascaded connection of N demultiplexing stages. The theoretical results obtained by analyzing the RF signal propagation through the sampling and demultiplexing stages were compared with the

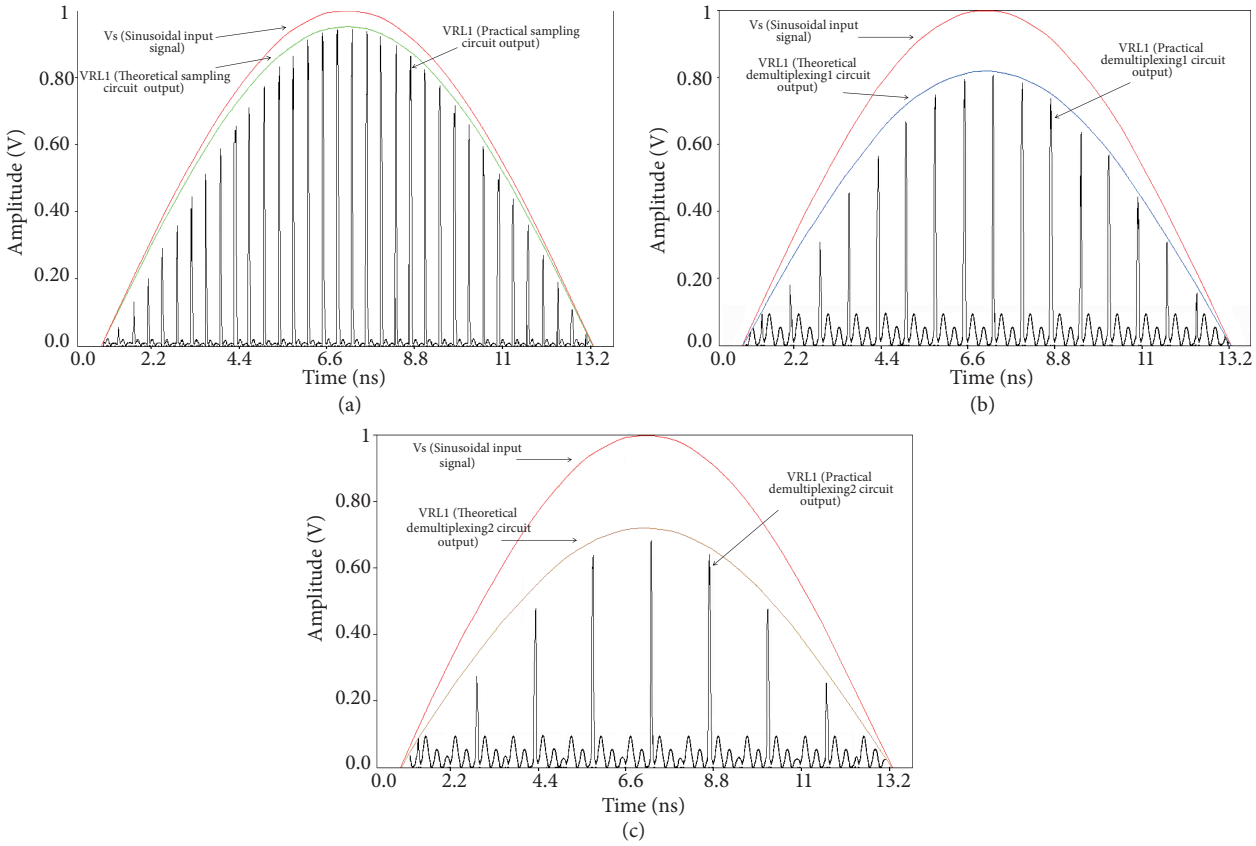

Figure 6. Measured outputs of the practical implemented circuit compared to the simulated transient response curves (40 MHz 300 mV peak sinusoidal input signal): a) outputs of the sampling circuit (2.5 GSPS), b) outputs of the first demultiplexing circuit (1.25 GSPS), c) outputs of the second demultiplexing circuit (625 MSPS).

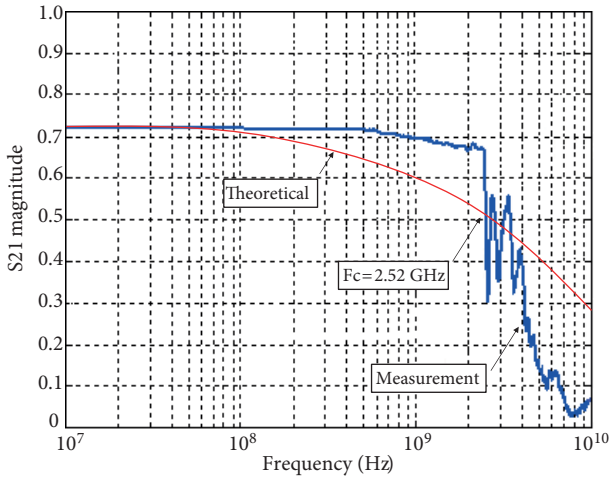

Figure 7. Frequency response of the sampling circuit with two demultiplexing stages.

measurements obtained from the optoelectronic sampling circuit connected in cascade with two demultiplexing stages implemented using commercial PIN-PDs. From the comparison, we found that the simulated transient response matched well with the sampled signals measured at the output of each stage. The measured signal

attenuation in each stage was consistent with the desired attenuation in the theoretical design. Hence, the analyzed scheme can readily be scaled to even higher sampling and demultiplexing rates by increasing the repetition rate of the optical pulses from the laser source and properly tuning the optical delay lines.

In addition, a theoretical curve of the frequency response obtained by plotting a Bode diagram from the transfer function of the sampling and demultiplexing circuit was compared with a measured curve obtained by using an S-parameter network analyzer. From the comparison, we observed that the measurement and the theoretical result obtained at the output of the second demultiplexing stage matched well at the cutoff frequency. Results obtained with the proposed theoretical scheme to calculate the cutoff frequency are consistent with practical measurements. As shown in Eq. (11), higher internal capacitance of the PIN-PD limits the dynamic response of the sampling circuit, reducing the response speed of the overall sampling and demultiplexing scheme. Hence, the limiting criteria to scale up this architecture are the availability of the required power and the switching speed of the PIN photodiodes.

Appendix

Procedure to calculate the load resistance of all stages (from R_{di} and R_{Ln}): the steps start from stage n and progress recursively. For stage n, $R_{LTn} = R_{Ln}$ for the previous stages; the parallel resistance with the adjacent stages must be taken into account.

Procedure:

Select the desired attenuation for each stage (from A_1 to A_n)

From $i = n$ to 1

For stage i, select the optical peak of the power to use P_i satisfying the restriction $P_i > P_{i+1}$

Using P_i, we obtain the I−V curve of the PIN-PDi

From the I−V curve of PIN-PDi, we select the operation point and obtain V_{di} and I_{di}

Compute I_{phi} and k_i

Compute R_{di} using Eq. (1)

Using A_i, compute the equivalent resistance R_{LTi} using Eq. (2)

Compute R_{Li} using Eq. (3)

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