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Comparative analysis of a novel topology for single-phase Z-source inverter with reduced number of switches

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Abstract: Z-source inverter has recently been introduced to overcome the limitations of conventional voltage source inverter. This paper deals with a novel topology of single-phase Z-source inverter (ZSI). This topology reduced the number of passive elements and active switches in order to make the inverter cheaper and smaller in size compared to traditional ZSI. Detailed analysis of the proposed topology is presented in this paper which includes calculations of boost factor, total harmonic disorder, magnitude of output voltage etc. Modulation technique used to control the switching of the proposed inverter is explained in detail. This paper also compares the proposed topology with conventional topologies of Z-source inverter. Simulation results of MATLAB and real-time simulators are shown to explain the working of the proposed topology.

Key words: Voltage source inverter, Z-source inverter, shoot-through state, LC-network

1. Introduction

Z-source inverter (ZSI) has many advantages over conventional voltage source inverters in terms of reliability, efficiency, cost etc. It uses a unique LC-impedance network to join the inverter with the power source [1]. Although this LC-network makes the inverter bulky, it also helps the inverter capable of providing a wide range of output voltage magnitudes. With the help of ZSI buck/boost operation can be performed without a transformer, which makes the system cheaper and more efficient. To carry out the boost operation, ZSI uses an additional state called shoot-through state in which both switches of the same-phase leg are turned on simultaneously. This shoot-through state is not possible in conventional VSI as it may damage the inverter. Hence, this property of ZSI to use shoot-through state makes it more reliable compared to the conventional VSI. However, there are certain drawbacks which are associated with the conventional ZSI. First, the conventional ZSI uses certain passive elements in its impedance network, which makes it quite bulky. To overcome this drawback, researchers have proposed many topologies which make use of less number of passive elements. One of these topologies is switched boost inverter which significantly reduced the number of passive elements but an additional switch is required for the operation of this inverter, which makes its control a bit complex and also with the increase in the number of semiconductor devices, the inverter circuit requires better protection compared to traditional ZSI [2]. L-Z source inverter is another inverter which does not use any capacitor for the boost operation; due to the absence of a capacitor, its cost and size decrease but it does not work well in discontinous conduction mode (DCM) [3]. The traditional ZSI does not draw continuous current from the

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input voltage source. To overcome this problem, embedded Z-source inverter (EZSI) was designed. Although EZSI draws continuous current from the source, it requires separate ground between the voltage source and the inverter circuit. Likewise, there are many topologies of Z-source inverter present in the literature with their advantages and problems. The power circuit diagram of conventional Z-source inverter is shown in Figure 1.

In this paper, a new improved topology of single-phase Z-source inverter is proposed which has significantly reduced the number of semiconductor switches and number of passive elements. By reducing them, the switching losses, cost, size, and weight are reduced and the efficiency of the inverter is improved. The switching frequency of the inverter is kept at fundamental frequency to further lower down the switching losses. Modulation technique used for the switching of the inverter is quite simple and is explained in detail in this paper.

2. Proposed topology

The proposed topology uses two inductors, i.e. L1 and L2, and one capacitor as part of the LC network. It has only two semiconductor switches unlike the conventional single-phase Z-source inverter, which uses four switches for single-phase configuration. There is no separate ground required between the voltage source and the inverter circuit. The proposed inverter works well in both discontinous conduction mode (DCM) and continous conduction mode (CCM). The circuit diagram for the proposed inverter is shown in Figure 2.

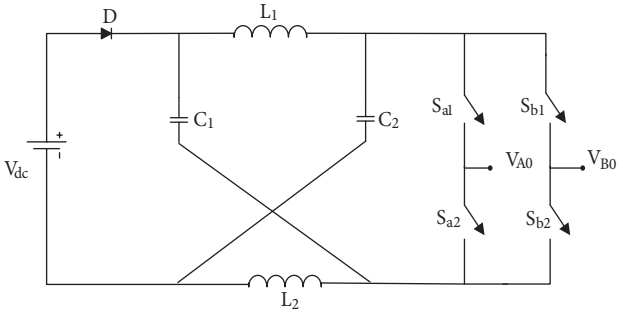

Figure 1. Conventional single-phase Z-source inverter.

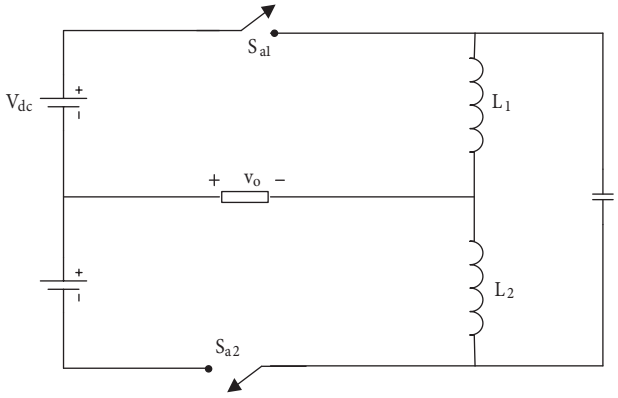

Figure 2. Proposed Z-source inverter topology.

3. Operating modes of the proposed inverter

The proposed topology has three modes of operation. The detailed analysis of modes of operations, along with switching states of the inverter, is explained in the section below.

3.1. The first operating mode

In this mode also known as the shoot-through state of the Z-source inverter, the two voltage sources used in the inverter charges the capacitor with switches S1 and S2 turned ON. The value of capacitor used in the inverter should be chosen with care as value of capacitor governs the current magnitude flowing through switches. It should be noted here that a very small amount of current also flows through both the inductors as well but the major portion of the current contributes to the charging current of the capacitor. The current through inductor increases as the charge on the capacitor increases. The charging current to the capacitor decreases to zero as the voltage level of capacitor equals the voltage level of DC voltage source. The charging current of capacitor in

this state is kept within limits by choosing the appropriate value of capacitor. The equivalent circuit diagram of the proposed inverter in this mode with current directions is shown in Figure 3.

3.2. The second operating mode

The proposed topology in this mode is shown in Figure 4. In this mode, the energy stored by the capacitor in the shoot-through state is transferred to the inductors for the steady-state operation of the inverter. In this mode, switch S1 is in ON state while S2 is kept in OFF state. During discharging of the capacitor, first the current through inductor increases but as the charge on the capacitor decreases, the current also decreases; hence, the polarity of inductor reverses and the effective voltage across load also increases. In this mode, only switch S1 is in ON state; therefore, a unidirectional current flows through the load.

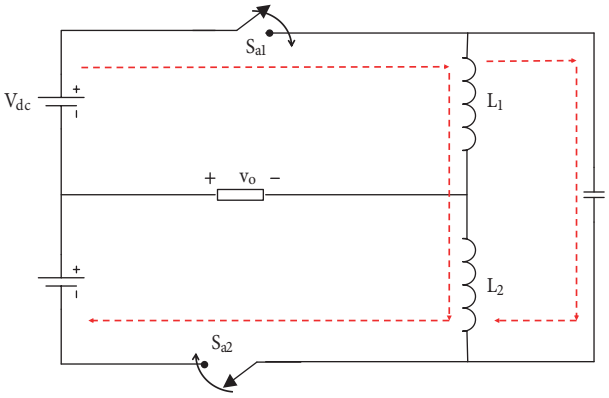

Figure 3. Proposed topology in mode 1.

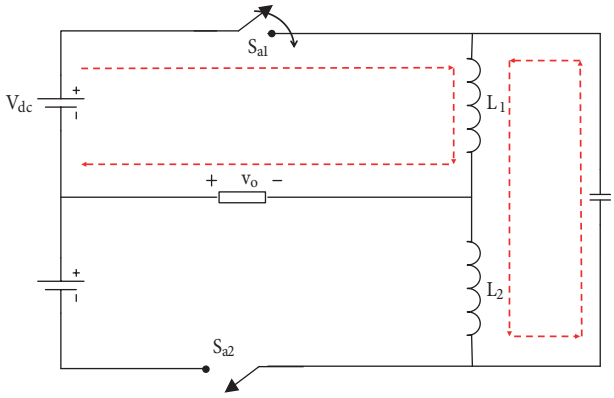

Figure 4. Proposed topology in mode 2.

3.3. The third operating mode

This mode is also the active mode of the inverter similar to the second operating mode; the only difference is that, in this mode, switch S2 will remain in ON state while switch S1 is in OFF state. Hence, the current flows in the opposite direction through the load compared to mode 2.

3.4. Boost factor calculation

Using KVL in shoot-through state:

$$v_{i_n} = V_L. \tag{1}$$

In active state:

$$V_0 = v_{i_n} - V_L, \tag{2}$$

where v_{i_n} is input voltage and V_L represents inductor voltage

From volt-sec balance for inductor, we have

$$v_{i_n}(\frac{D_{S_T}}{2}) + (v_{i_n} - V_0)\frac{(1 - D_{S_T})}{2} = 0 \tag{3}$$

$$V_0 = \frac{1}{(1 - D_{S_T})} v_{i_n} \tag{4}$$

$$B = \frac{1}{(1 - D_{S_T}),} \tag{5}$$

where B is Boost factor and D_{S_T} represents shoot-through duty ratio.

3.5. RMS value of the output voltage

The output voltage wave of the inverter is nearly sinusoidal if shoot-through duty ratio should be kept low. The RMS value of the output voltage wave is calculated as follows:

$$V_{R_{M_S}} = \sqrt{\left(\frac{2}{T}\left(\int_{T.D_{S_T}/2}^{T/2} (Asin\omega\ t)^2 dt + \int_{T/2+T.D_{S_T}/2}^{T} (Asin\omega t)^2 dt\right)\right)}, \tag{6}$$

$$V_{R_{M_S}} = A\sqrt{\frac{(1-D_{S_T})}{2}}, \tag{7}$$

also,

$$\omega = \frac{2\pi}{T(1-D_{S_T}),} \tag{8}$$

where A is the maximum amplitude of output voltage wave which depends on the value of the capacitor, and D_{S_T} is shoot–through duty ratio.

4. Performance characteristics

In this section, certain important performance characteristics such as variation of boost factor and output voltage with shoot-through duty ratio, (total harmonic disorder) THD variation with boost factor, and capacitor voltage stress for the proposed topology are discussed.

4.1. Boost factor and shoot-through duty ratio variation

From Figure 5, it is observed that boost factor increases with shoot-through duty ratio. With the increase of shoot-through duty ratio, the capacitor holds the charge for a longer duration and remains at input voltage level during shoot-through interval.

The shoot-through duty ratio for the proposed inverter may be increased till certain limit viz. $D_{S_T} = 0.5$. If this limit is exceeded, the system may become unstable. This limitation is observed in most topologies of single-phase Z-source inverter.

4.2. Output voltage waveform variation with shoot-through duty ratio

It is observed from Figure 6 that with the increase in shoot-through duty ratio the magnitude of output voltage and therefore the boost factor increases. But as the boost factor increases, the output voltage wave moves away from pure sinusoidal wave. During the shoot-through state of the inverter, the voltage across the inductor is equal to the input voltage; therefore, there is no potential difference across the load terminals. Since the duration of zero level interval is very short, it does not affect the performance of the inverter much. Figures 7 and 8 show the output voltage with shoot-through ratios 0.1 and 0.2, respectively.

4.3. Boost factor and THD variation

From Table 1, it can be concluded that with the increase in shoot-through duty ratio, boost factor and THD for the proposed topology increase. The value of shoot-through duty ratio can be decided from the application whether the power quality or the voltage magnification is more important. Hence, there is a trade-off between the boost factor and THD of the output voltage wave. The harmonic spectrum of the output voltage for different shoot-through duty ratios is presented in Figures 9 and 10.

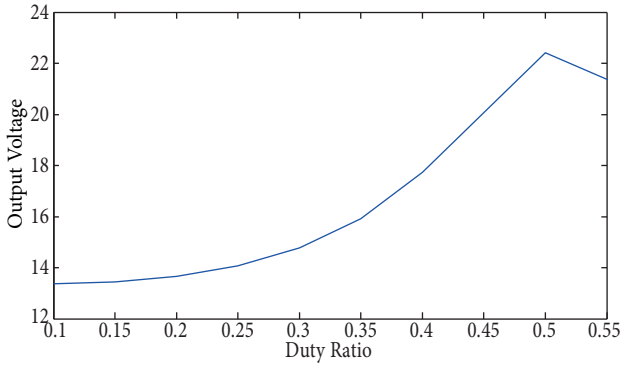

Figure 5. Variation of output voltage with shoot-through duty ratio.

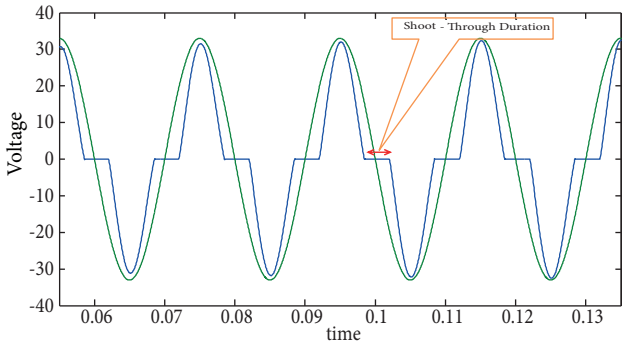

Figure 6. Comparison of output voltage with pure sinusoidal wave.

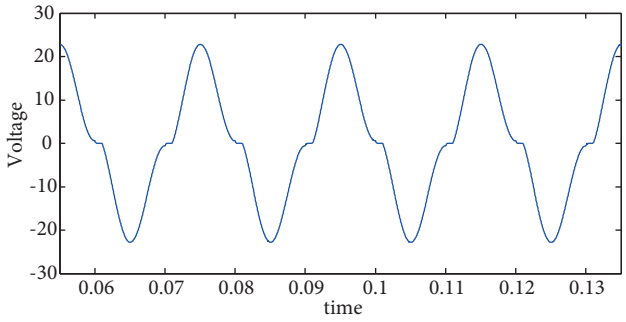

Figure 7. Output voltage with shoot-through duty ratio $D_{S_T} = 0.1$.

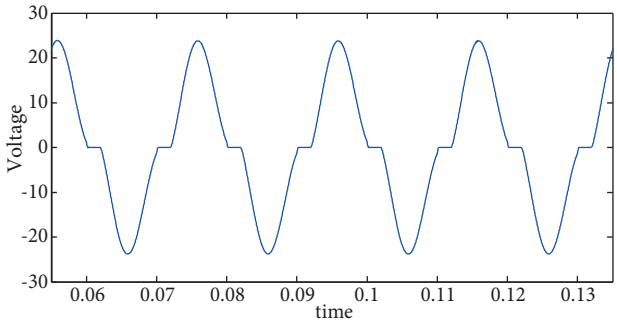

Figure 8. Output voltage with shoot-through duty ratio $D_{S_T} = 0.2$.

Table 1. Variation of boost factor and THD of the proposed inverter with shoot-through duty ratio.

D_{S_T}	0.04	0.1	0.2	0.3	0.4	0.5
B (%)	7.58	11.41	13.83	23.16	47.7	86.75
THD (%)	13.4	13.4	20.2	28.7	40.3	43.54

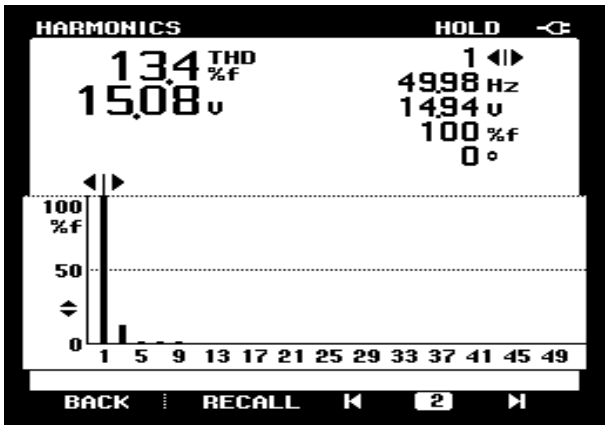

Figure 9. Harmonic spectrum of output voltage with ST duty ratio $D_{S_T} = 0.1$.

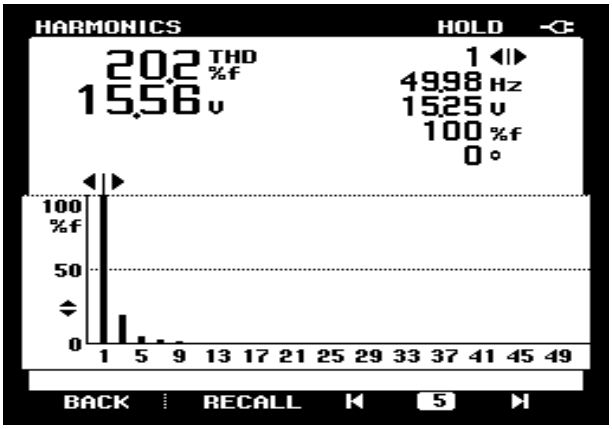

Figure 10. Harmonic spectrum of output voltage with ST duty ratio $D_{S_T} = 0.2$.

4.4. Capacitor voltage stress

Capacitor voltage stress is also given the utmost importance in the case of ZSI as the rating of capacitor plays an important role in determining the overall size and weight of the inverter. There are many topologies suggested in the literature to minimize the voltage stress of the capacitor used in ZSI such as Q-ZSI in which the voltage stress across the capacitors is reduced to a great extent so that the cost of the inverter can be reduced. From Figure 11, it can be observed that with the increase in the shoot-through duty ratio, the capacitor voltage stress also increases.

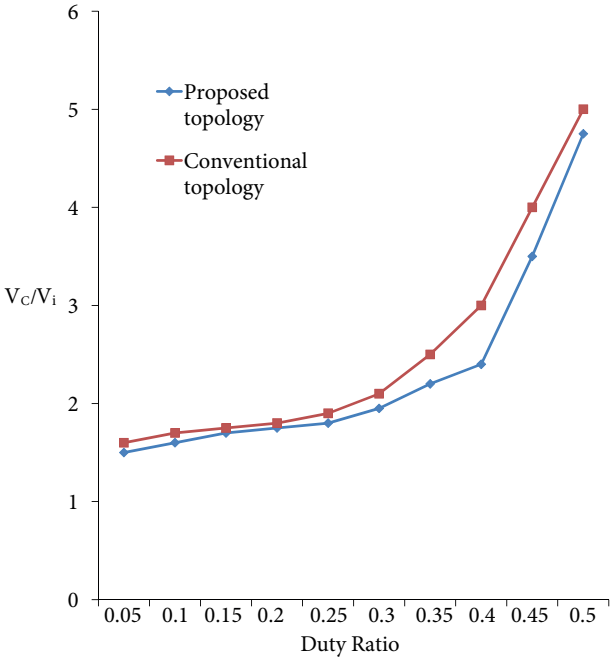

Figure 11. Variation of (V_C/V_i) with shoot-through duty ratio.

4.5. Efficiency

Efficiency of the proposed inverter is quite high compared to most of the conventional topologies due to reduced losses. Inverter losses include on-state conduction loss and switching loss but here, due to lower number of switches, these losses are greatly reduced. Moreover, the switching frequency is also quite low which further lowers down the switching losses. Figure 12 below shows the efficiency of the inverter with variation in shoot-through duty ratio.

5. Modulation technique

The logical diagram to generate the control signals for the switches and control signals of the modulation technique are given in Figures 13 and 14, respectively.

The switching technique used for the proposed topology is the same as that used for high-voltage-gain switched boost inverter which requires comparators and logic gates [4,5]. As the proposed topology has only two switches, only two control signals are required here. A triangular signal ($V_{t_{ri}}$) is compared with two constant signals $V_{S_{T_1}}$ and $V_{S_{T_2}}$. $V_{S_{T_1}}$ is signal which is decided directly by the shoot through duty ratio (D_{S_T}) and $V_{S_{T_2}}$ = 1-D_{S_T}. Signal U is generated by comparison of the sinusoidal signal with zero value, while U' represents the

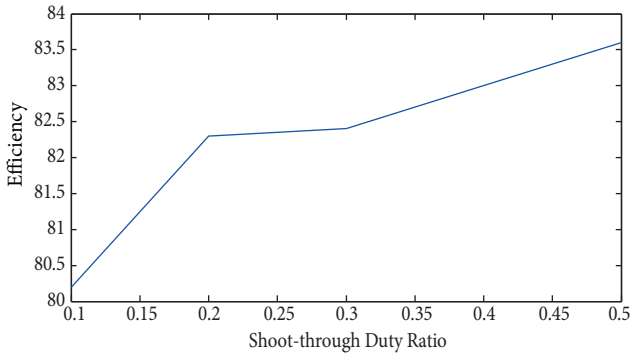

Figure 12. Variation of efficiency with shoot-through duty ratio.

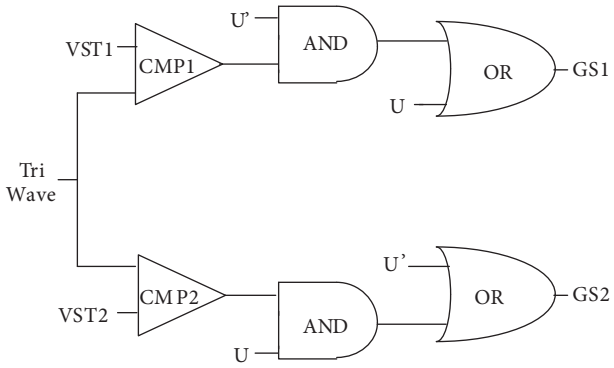

Figure 13. Logical diagram for generating gate signals.

negation of U. The switching technique presented here is simple and easy to implement with very short delay time. Moreover, with the help of this technique, the frequency of the output voltage wave can be controlled easily. The switching frequency for the proposed inverter is chosen to be 50 Hz. The biggest advantage of low switching frequency is less switching losses and it also maintains constant shoot-through duty ratio which helps the inverter to perform better. Since the duty ratio decides the boost factor, it may be varied to control the magnitude of the output voltage.

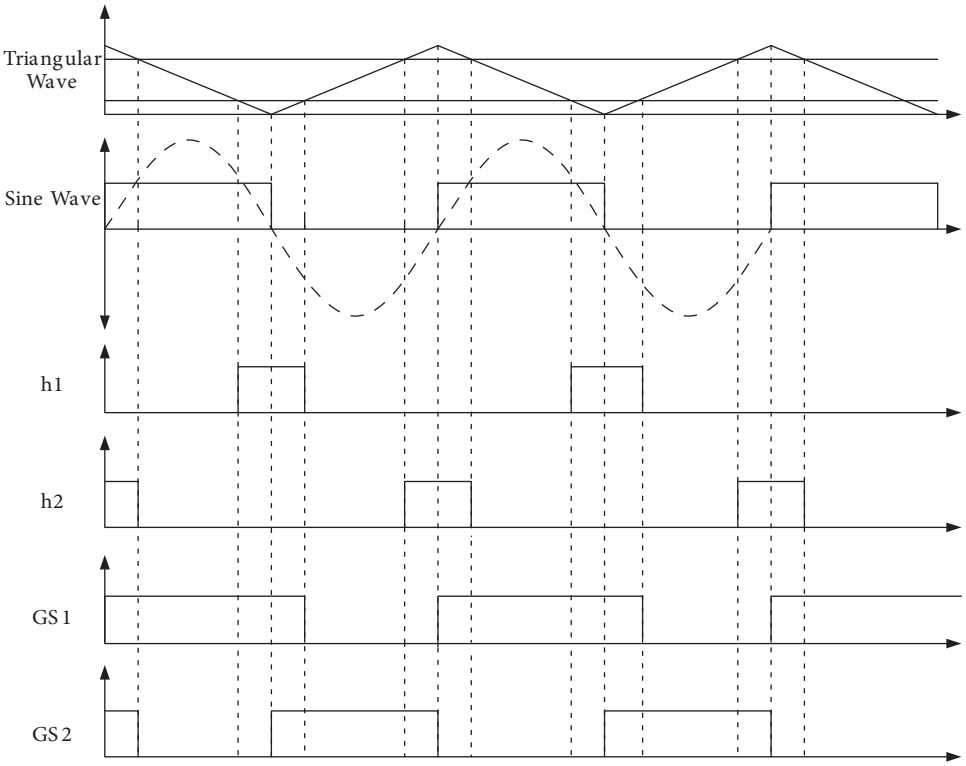

Figure 14. Control signals and main waveforms.

6. Simulation results

Simulation results with MATLAB and real-time simulators are shown in the section below to explain the performance of the proposed inverter.

6.1. Simulation results with MATLAB

The proposed topology was simulated to observe its performance characteristics under different loading conditions. The main emphasis is given to the variation of capacitor current and boost factor with shoot-through duty ratio.

Figure 15 shows the capacitor voltage waveform with shoot-through duty ratio of 0.2. The input voltage source is kept at 12 V. It can be observed that during shoot-through, the capacitor voltage stays at input voltage level. In active state, it transfers its power to the inductor; therefore, the capacitor current decreases. The equations governing the states of the inverter are as follows:

$$V_L = L\frac{di}{dt} \tag{9}$$

$$i_C = C\frac{dV}{dt} \tag{10}$$

Using KVL during active state,

$$V_L + V_C = 0, \tag{11}$$

$$I_L + I_c = 0. \tag{12}$$

The above equations result in the second-order differential equation

$$\frac{d^2V_c}{dt^2} + \frac{V_C}{LC} = 0 \tag{13}$$

Solving Eq. (13), we get

$$V_C = Asin\ \ (\omega t + \alpha), \tag{14}$$

$$I_L = I_C = AC\ cos\quad (\omega t + \alpha), \tag{15}$$

where

$$A = \sqrt{(V_{c_i})^2 + \left(\frac{I_{L_i}}{(\omega C)}\right)^2} \tag{16}$$

and

$$= arctan\left(\frac{\omega C V_{c_i}}{I_i}\right). \tag{17}$$

However, during the shoot-through state

$$V_C = v_{i_n}, \tag{18}$$

where v_{i_n} is the input voltage.

Figure 16 shows the capacitor current of the inverter. It is observed that during the shoot-through state, the current through the capacitor is at zero value.

Figure 17 shows the output voltage waveform of the inverter. It can be observed that the output voltage remains at zero level for finite duration during the shoot-through period. The increment in the shoot-through duty ratio results in higher voltage magnification but it also leads to higher THD.

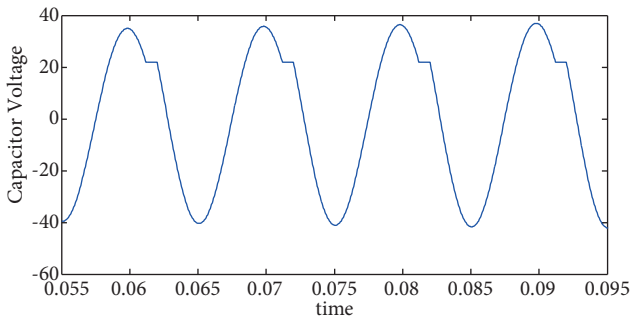

Figure 15. Capacitor voltage of the proposed inverter with $D_{S_T} = 0.2$.

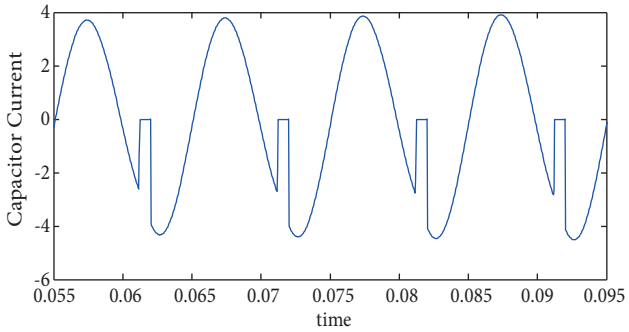

Figure 16. Capacitor current of the proposed inverter for $D_{S_T} = 0.2$.

6.2. Simulation results with real-time simulator

Real-time simulation results were obtained for the proposed topology using dSPACE 1104 and OPAL-RT Simulator OP5700. dSPACE was used to generate the control signals for the switches of the inverter. The real-time results show the variation of output load voltage, capacitor voltage, capacitor charging current, and inductor voltage waveforms for different duty ratios. The shoot-through duty ratio was also varied to observe the variation of boost factor and THD. Figures 18 and 19 show the variation of output voltage, capacitor voltage, capacitor current, and inductor voltage for shoot-through duty ratio equal to 0.2 and 0.3, respectively. The results from real-time simulator are quite similar to those obtained with MATLAB. It can also be observed that the frequency of capacitor voltage is twice compared to the frequency of output voltage. Figure 19 shows the output voltage and current of the proposed inverter.

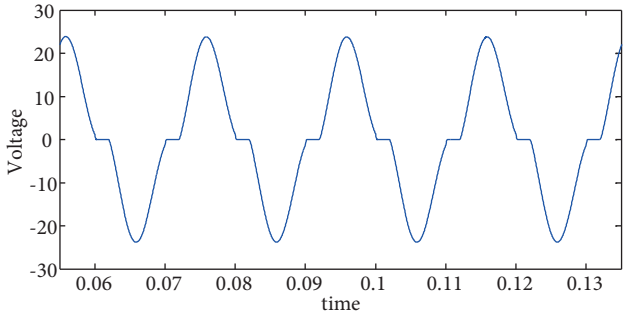

Figure 17. Output voltage of the inverter for $D_{S_T} = 0.2$.

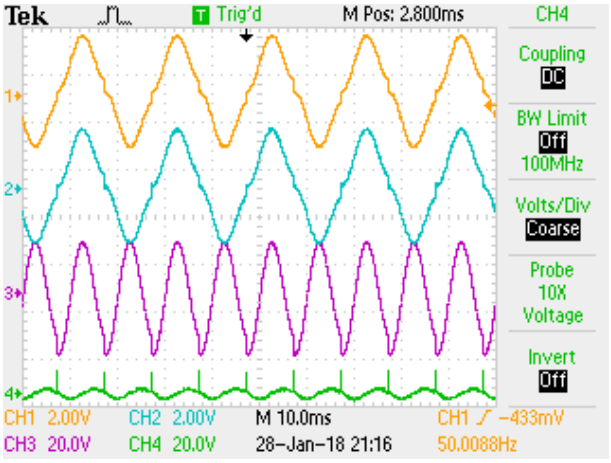

Figure 18. Variation of different parameters for duty ratio $D_{S_T} = 0.2$.

7. Comparison of the proposed topology with the conventional Z-source inverter

Apart from the lower number of switches, the proposed topology has lower number of passive elements count than the conventional Z-source inverter. The conventional Z-source inverter contains one extra capacitor compared to the proposed topology which helps in reducing the cost and overall size of the inverter. Also the magnitude of the capacitor used in the proposed topology is much lower than that used in the conventional inverter.

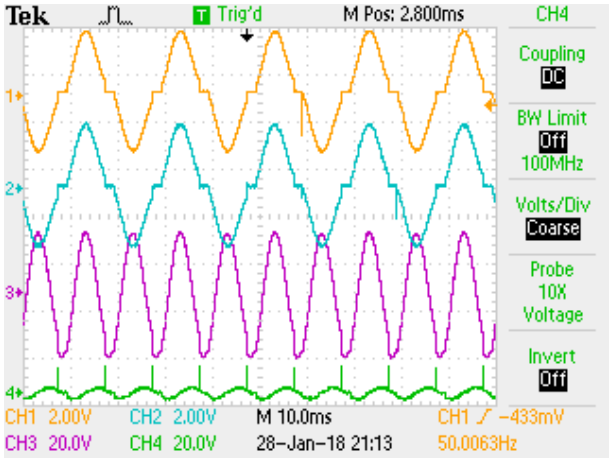

Figure 19. Variation of different parameters for duty ratio $D_{S_T} = 0.3$.

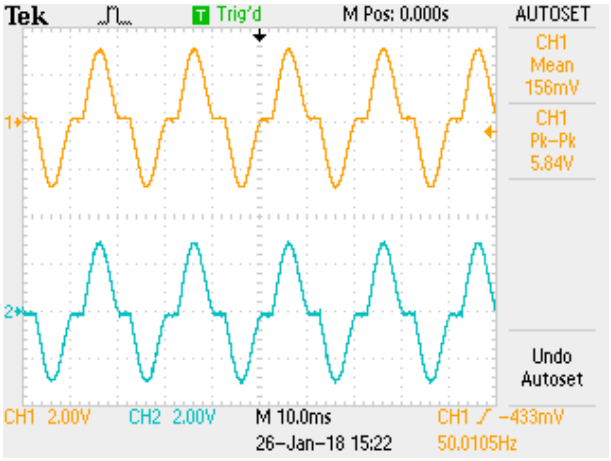

Figure 20. Output voltage and current of the proposed inverter with ST duty ratio $D_{S_T} = 0.2$.

Lower magnitude of capacitance helps in reducing the magnitude of the inrush current which is observed at the start of shoot-through state [6]. Table 2 shows the comparison of the proposed topology with other Z-source inverter topologies. The switching frequency used for the conventional single phase Z-source inverter is of the order of 10 KHz but the switching frequency for the proposed topology is chosen to be 50 Hz; hence, lower switching losses are observed in the proposed topology. However, the on-state conduction losses in the case of low switching frequency are somewhat higher but the major losses are caused due to high switching frequency [7]. Table 3 shows the comparison of the proposed topology with the conventional Z-source inverter in terms of different parameters. Modulation technique used for switching of inverter is simple and easy to implement. There are plenty of modulation techniques available for the switching of conventional Z-source inverter but several techniques do not maintain the constant shoot-through duty cycle which may affect the performance of the inverter but the modulation technique presented in this paper does maintain the constant duty ratio which

Table 2. Comparison of the conventional ZSI topologies and the proposed topology.

Topology	L	C	Switches	Diodes	B
Proposed topology	2	1	2	0	$1/(1-D_{S_T})$
ZSI [1]	2	2	4	5	$1/(1-2D_{S_T})$
SBI [2]	1	1	5	1	$(1-D_{S_T})/(1-2D_{S_T})$
LZSI [3]	2	0	4	3	$(1+D_{S_T})/(1-D_{S_T})$
HB-SBI [4]	2	2	4	6	$(1-D_{S_T})/(1-$ 3D $_{S_T})$

Table 3. Parameters used for comparison of ZSI and the proposed topology.

Parameter/Component	Conventional ZSI	Proposed ZSI
Switching frequency	10 KHz	50 Hz
Capacitor value	200μ F	150μ F
Inductor value	5 mH	7.5 mH
Passive elements	2L,2C	2L,1C
Active elements	4	2

can be altered easily as per the requirement of the output voltage [8–10]. There are also some limitations of the proposed topology compared to other conventional topologies such as high in-rush current at the start-up due to presence of capacitor but this problem can be eliminated with a suitable method suggested in the literature.

8. Conclusion

This paper presents a novel topology of single-phase Z-source inverter which uses less number of switches compared to the conventional Z-source inverter. The modulation technique used for the proposed topology is explained in detail. It is quite simple to implement with switching frequency set at fundamental frequency, i.e. 50Hz., which may significantly reduce the cost, size, and weight with improved efficiency. Various parameters, such as boost factor, THD, and capacitor voltage stress, were calculated and results from MATLAB and real-time simulators are also presented.The proposed topology was compared with some conventional Z-source inverter topologies in detail in terms of various parameters which included the number of active elements, passive elements, boost factor etc.

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