Tunable Class-F high power amplifier at X-Band using GaN HEMT

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Received: 11.03.2018 • Accepted/Published Online: 26.07.2018 • Final Version: 28.09.2018

Abstract: Class-F type amplification stands on proper termination of harmonics such as short for even harmonics and open for odd harmonics. Moreover, termination of only the first few harmonics is practical for high-frequency circuits, while obtaining satisfactory short and open terminations at high frequencies is a challenging design issue. In the present study, a topology of harmonics termination for Class-F load network with 2nd and 3rd harmonics and its relative analytical analysis are presented. The proposed output termination structure for Class-F type amplification provides an improved short termination of 2nd harmonic; therefore, the efficiency of the power amplifier increases. In addition, the topology implemented with the microstrip lines has a tunable structure, and it is suitable for very high-frequency applications due to its straightforward architecture. An X-Band high power amplifier for a small satellite transmitter is designed and fabricated with the proposed method. A 0.25 μm GaN on SiC HEMT having a total gate width of 1.25 mm is used. The PA achieves the peak PAE of 55% at 8.1 GHz while the output power is 36 dBm at the 3 − dB compression point. The Class-F PA has higher than 50% PAE and 35.5 dBm output power in the band of 7.9 − 8.2 GHz. The measured linear power gain is 16.2 dB.

Key words: Class-F, gallium nitride, high-electron-mobility transistor, X-Band, power amplifier, satellite communication

1. Introduction

A high power amplifier (HPA) is usually the most power consuming subsystem of a transmitter. Therefore, high efficiency is a desired specification for an HPA not only to reduce the total power consumption but also to increase the lifetime and reliability of the system. There are several HPA classes for microwave applications achieving high efficiencies such as Class E, F, J, and S. Each of them has some advantages and disadvantages regarding the circuit complexity, implementation difficulties, bandwidth limits, output power capability, etc.

The load network of a Class-F amplifier is a current and voltage waveform shaping circuit applying short and open circuit termination at the drain node for even and odd harmonics, respectively, at the same time. Shaping the current and voltage waveforms by manipulating the harmonics results in a squarish voltage and half-sinusoidal current waveforms at the drain. Therefore, the overlaps between the voltage and current decrease at the drain node. This situation decreases the power dissipation on the transistor and increases the efficiency of the amplifier.

Although terminating all harmonics can provide 100% theoretical efficiency, it is not realistic in real-world microwave circuits because the increased complexity and physical size of the circuit cause increment

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in the insertion and radiation losses [1, 2]. In addition, the drain-source capacitance (\(C_{ds}\)) prevents proper terminations required for high order harmonics [3, 4]. Therefore, a load termination up to 3rd harmonics is convenient and feasible for high-frequency HPAs. In theory, it provides an efficiency of up to 81.7% [1, 2].

There are various reported Class-F output networks for various power levels and operating frequencies in order to obtain a proper termination of the harmonics to achieve high efficiency. Class-F type amplifiers are also convenient to achieve satisfying efficiency and output power performances at very high frequencies such as X and Ku Bands due to practical and sufficient load termination structures. On the other hand, the parasitic and nonlinear effects of a transistor caused by output capacitance, bonding pads, contact resistance, soldering, etc. have a significant influence on the termination networks, especially at very high frequencies. Moreover, the nonlinear transistor models generally do not enclose and are not accurate enough to predict the effects of the parasitic components at the frequencies of the harmonics. Therefore, the PAs consisting of waveform shaping termination networks usually require fine-tuning to achieve optimum performance after fabrication.

The short communication window of small low earth orbit (LEO) satellites requires high frequency and wideband communication systems. The use of X-Band downlink systems has become popular in small satellites due to the improvements in solid-state device technologies [5]. For instance, the GaN HEMT devices can provide better performance for high power applications due to their promising electrical specifications, thermal conductivity, and small size in the desired frequency range for high data rate small satellite transmitters.

The Class-F load network topology proposed by Tsang [6] is suitable for high-frequency applications and mechanical tuning after fabrication. However, the proposed network does not provide a satisfying 2nd harmonic termination for an improved Class-F termination. Therefore, in the present study, the proposed topology is modified and enhanced to obtain improved short termination at 2nd harmonic. The analytic relations and design methodology of the proposed new structure are presented. Furthermore, open-stub based structures are used in load and matching networks, providing the possibility of tuning in the case of unpredictable nonlinearity issues of the transistor and tolerance of other components. Later, the new topology is implemented to a high power amplifier realized with a GaN-on-SiC HEMT having a total gate width of 1.25 mm (10 × 125 µm) at X-Band. The space-qualified components and materials are considered during the design. The fabricated circuit is tested and measured as an SMA connectorized module.

The designed and implemented Class-F amplifier delivers an output power of 36 dBm at 8.1 GHz at the 3 – dB compression point (\(p_{3dB}\)) while the power added efficiency (PAE) is 55%. The measured linear power gain is 16.2 dB. In the 400 MHz bandwidth, the PA shows more than 50% PAE and less than 1 dB gain ripple.

In section 2, the structure, analytical analysis, and simulation results of the proposed load network of the Class-F topology are presented. The design details, layout, and measurement results of the fabricated amplifier are shown in section 3.

2. Analysis of the Class-F load network

The proposed Class-F load network includes a proper termination of the 2nd and 3rd harmonics. Figure 1 shows the schematic diagram of the output circuit of the designed Class-F load network providing a short termination at the 2nd harmonic and open termination at the 3rd harmonic. The current and voltage waveforms are manipulated by only 2nd and 3rd harmonics not to increase the circuit complexity and insertion loss of the load network. The components coded in the diagram as A, B, C, and D represent transmission lines.

In Figure 1, transmission line A, the first element of the load network from transistor to output, is a
Impedance Matching @fo

\( \frac{3}{4} \lambda \)

3 / 4

1 / 4

VDD

A

B

C

(2fo→ short, 3fo→ open)

3fo, short

fo, open

2fo, short

Z_{Load}

Z_C

Z_B

Z_T

D Z_D

\( \frac{1}{4} \lambda \)

Figure 1. Purposed structure of the Class-F load network.

quarter wavelength transmission line at a 3rd harmonic frequency (\( \frac{3}{4} \lambda \)), followed by an open stub Line B providing an open circuit at 3fo. Line D, i.e. a quarter wavelength at fo (\( \frac{1}{4} \lambda \)), acts as an RF short at fundamental frequency fo. Therefore, Z_D impedance is open for fo and short for 2fo at the same time. Impedance values of the Z_C, Z_B, Z_T, and Z_{Load} are defined at 2fo as

\[
Z_C = jZ_oC \tan(\beta_2 l_C). \tag{1}
\]

\[
Z_B = -jZ_oB \cot(\beta_2 l_D). \tag{2}
\]

\[
Z_T = Z_B \parallel Z_C. \tag{3}
\]

\[
Z_{Load(2fo)} = \frac{Z_T + jZ_oA \tan(\beta_2 l_A)}{Z_oA + jZ_T \tan(\beta_2 l_A)}. \tag{4}
\]

In Eqs. (1)–(4), Z_{oA}, Z_{oB}, Z_{oC} are the characteristic impedance of the lines, while \( \beta_2 \) is \( 2\pi/\lambda_2 \), and \( l_A \) and \( l_B \) are \( \lambda_2/6 \) (\( \frac{3}{4} \lambda \)). A short termination of Z_{Load} at 2fo is required to achieve a proper Class-F load termination for the 2nd harmonic. Eq. (5) shows that there is a solution to find the optimum length of the transmission line C to obtain a short termination at the 2nd harmonic frequency 2fo.

\[
l_C = \frac{1}{\beta} \arctan \left( \frac{Z_{oA}Z_{oB} \tan(\beta_2 l_A) \cot(\beta_2 l_B)}{Z_{oC}(Z_{oA} \tan(\beta_2 l_A) - Z_{oB} \cot(\beta_2 l_B))} \right). \tag{5}
\]

The electrical length of Line C (\( l_C \)) is set to 0.11 \( \lambda_2 \), which provides Z_{load} to short out at 2fo while the characteristic impedances Z_{oA}, Z_{oB}, and Z_{oC} are 50 Ω. In Figure 2, implementation of the designed circuit with ideal transmission lines and microstrip lines, and the simulation results of impedances at 2fo and 3fo are shown. Although the microstrip line based load network cannot provide a perfect short due to the substrate and metal layer losses, it is acceptable for practical applications.
3. Implementation and measurement results

A single bare die GaN HEMT with 1.25 \text{ mm} total gate width (10 \times 125 \text{ \mu m}) is selected by considering its power gain and output power capability regarding the requirements of the satellite transmitter. The drain voltage is set to 28 \text{ V} and \( I_{dq} \) is 125 mA. The circuit is implemented on a high thermal conductivity substrate (RT/Duroid 6035HTC, \( h = 0.508 \text{ mm} \), \( \epsilon_r = 3.5 \), \( \text{loss tangent} = 0.0013 \)), which is also qualified for the LEO missions.

A nonlinear model of the transistor, which is supplied by the manufacturer, is used for the design and nonlinear analysis. After the designing of the load network with microstrip lines, a load-pull simulation is performed including the Class-F load network to find the impedances for optimum efficiency and power at operating frequency. The parasitic effects and intrinsic components such as bonding pads and \( C_{ds} \) capacitance should be considered carefully to obtain a proper and desired termination. However, an extraction process is not possible to observe real waveforms at the drain due to the restrictions of the nonlinear transistor model. Hence, a detailed time domain analysis to observe the current and voltage waveforms at the current source of the transistor is not feasible to confirm the Class-F type of termination.

Therefore, an EDA-tool based optimization for fine-tuning is performed together with the transistor by considering the efficiency and output power to achieve the best performance. After the optimization, an EM simulation is performed by AWR Axiem to verify the design. The input and output structures including the metal box in accordance with space requirements are simultaneously simulated. Moreover, several trace extension pads are also placed after the open stubs to have tuning flexibility after fabrication. Figure 3 displays the layout of the final circuit and Table 1 presents its design parameters.

The fabricated printed circuit board (PCB) is placed into a metal package where the gate and drain pads of the transistor are connected to PCBs with the diameter of 38 \text{ \mu m} Au bonding wires. The AuSn (80/20) material is used for soldering of the transistor to increase thermal conductivity instead of conductive epoxy. The dimensions of the final amplifier are 40 \text{ mm} \times 37.7 \text{ mm} \times 11 \text{ mm}. The total weight is 93 g.

At first, the stability of the PA is verified under small signal condition. An active load-pull system is used to measure the performance and to tune the implemented PA. Some physical and electrical tuning is applied to
Detailed layout of the designed input and output circuits.

Table 1. The lengths and widths of the microstrip lines, angles, and radii of the radial stubs on the circuit given in Figure 3.

<table>
<thead>
<tr>
<th>Part</th>
<th>Length (mm)</th>
<th>Part</th>
<th>Length (mm)</th>
<th>Part</th>
<th>Width (mm)</th>
<th>Part</th>
<th>Electrical Length</th>
<th>Part</th>
<th>Radius (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>5.00</td>
<td>L8</td>
<td>2.99</td>
<td>W1</td>
<td>1.11</td>
<td>Rd1-θ</td>
<td>90.0°</td>
<td>Rd1-r</td>
<td>3.93</td>
</tr>
<tr>
<td>L2</td>
<td>6.63</td>
<td>L9</td>
<td>3.94</td>
<td>W2</td>
<td>0.40</td>
<td>Rd2-θ</td>
<td>41.6°</td>
<td>Rd1-r</td>
<td>1.70</td>
</tr>
<tr>
<td>L3</td>
<td>3.58</td>
<td>L10</td>
<td>1.55</td>
<td>W3</td>
<td>0.60</td>
<td>Rd3-θ</td>
<td>34.4°</td>
<td>Rd1-r</td>
<td>2.51</td>
</tr>
<tr>
<td>L4</td>
<td>2.82</td>
<td>L11</td>
<td>0.89</td>
<td>W4</td>
<td>0.60</td>
<td>Rd4-θ</td>
<td>70.0°</td>
<td>Rd1-r</td>
<td>2.12</td>
</tr>
<tr>
<td>L5</td>
<td>5.54</td>
<td>L12</td>
<td>5.69</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L6</td>
<td>3.00</td>
<td>L13</td>
<td>5.10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L7</td>
<td>8.50</td>
<td></td>
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<td></td>
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achieve the best performance by considering iteratively the active load-pull measurements and simulations. The open stub L8 is extended with bonding wires, the open stub L9 is shortened, and the radial stub Rd3 is removed. The 2.2 \(pF\) capacitor at the gate is replaced with a 1.8 \(pF\) capacitor. The quiescent current is reduced to 110 \(mA\). One of the bonding wires at the drain is removed to increase the inductance between the load network and drain pad. An additional bonding wire is attached to the gate to reduce the total inductance between the input matching network and gate pad. Figure 4 presents the final view of the amplifier with modifications. Figure 5 shows a photograph of the amplifier with connectors and biasing pins.

Figure 6 shows the measured and simulated S-parameters. Figure 7 depicts the power gain and PAE versus output power at 8.1 \(GHz\). The implemented PA has 16.2 \(dB\) linear power gain. The saturated power and peak \(PAE\) at the \(3dB\) are 36 dBm and 55\% at 8.1 \(GHz\), respectively. The measured output power is 1 \(dB\) and the measured \(PAE\) is 1.5\% less than the simulation. On the other hand, the presented measurement data
are achieved after several tuning processes. Therefore, it indicates that the nonlinear model of the transistor is convenient to predict the feasible performance values such as output power, gain, and efficiency; however, the simulated input and output impedance values of the fundamental and harmonics frequencies are not accurate enough to obtain a suitable load and matching networks for a first-pass design. Figure 8 presents the measured wideband response of the $PAE$, output power, and compressed power gain at $p3dB$. The PA achieves higher than 50% efficiency and less than 1 $dB$ gain ripple between 7.88 and 8.27 GHz band.

The results show that designed Class-F HPA provides high efficiency in the bandwidth of 400 MHz. In Table 2, a comparison of similar and the latest GaN amplifiers at the X-Band consisting of transistors with 0.25 $\mu m$ gate length is presented.

4. Conclusion

The topology described in this article is proposed to improve the performance of a Class-F amplifier output termination network for 2nd and 3rd harmonics. The proposed architecture's parametric and reduced complexity also provides an opportunity for optimization during the design, and a possibility of mechanical tuning after
implementation to compensate for the unpredictable effects of the parasitic and nonlinear components. The Class-F load network is implemented to design a power amplifier using a GaN HEMT with discrete components. The measured results indicate that the proposed structure is convenient to apply also very high operating frequency amplifiers.

The power amplifier is assembled into a metal box and ready to use as an HPA module with SMA connectors. The measurements reveal that peak PAE of 55% and peak output power of 36.5 dBm are achieved at $p3dB$. The PA has 16.2 dB linear gain and also represents higher than 50% efficiency with almost 400 MHz bandwidth.

Acknowledgments

This study was supported by İstanbul Technical University (Grant Number 37348), and TÜBİTAK 2211/A and 2214/A programs. The authors would like to acknowledge the support of Saito Laboratory at the Japan Aerospace Exploration Agency (JAXA) Sagamihara Campus.

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