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An RC-triggered ESD clamp for high-voltage BCD CMOS processes

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Abstract: This paper presents a novel RC-triggered, field-effect transistor (FET)-based power clamp that can be used in high-voltage complementary metal oxide semiconductor (CMOS) processes. A simple two-stage design provides a fast trigger while keeping the clamp transistor on for much longer than the triggering duration without the need for an additional digital latching circuit. As the presented technique does not require any digital circuits, it is especially useful in bipolar-CMOS-DMOS (BCD) processes, where the implementation of digital blocks is difficult due to the limited gate-to-source voltage of the laterally diffused metal oxide semiconductor (LDMOS) transistors. The proposed architecture is implemented in a 0.25-μm BCD process offered by TSMC. Simulation results show that Class 3A-level electrostatic discharge (ESD) protection can be achieved with an 8-mm-wide device while keeping all gate-to-source voltage values below the recommended 5-V limit. As the circuit operation depends on the well-modeled transient behavior of transistors, the proposed technique can be extended to other ESD ratings and can also be migrated to other processes without the need of extensive hardware verification.

Key words: RC-triggered clamp, BCD CMOS, high-voltage CMOS, ESD protection

1. Introduction

With the increasing need of smart power management systems, semiconductor foundries have started to offer legacy complementary metal oxide semiconductor (CMOS) technologies with new options and features such as high-voltage (HV) MOS and bipolar transistors. Some of these processes achieve HV handling with thick gate oxide thickness. In such processes, the threshold voltage of HV transistors is high, and thus the current drive capabilities are low [1,2]. To mitigate the low current drive and large threshold voltage problem, many companies offer HV transistors with standard oxide thickness [3]. Such HV transistors can withstand very high drain-to-source (V_{DS}) voltages (e.g., 40 V), whereas their gate-to-source (V_{GS}) voltage values are limited to those of low voltage devices (e.g., 5 V) for reliable operation. Because of the limited V_{GS} voltage, care must be taken in circuit design to ensure that the gate-to-source voltage of such devices is kept below the maximum operating voltage through the use of circuit techniques and clamping devices. This limitation prevents the HV devices from being used in building even simple digital blocks, such as inverters, without significant static power dissipation. This is generally acceptable since digital functionality is better built by low voltage devices in a much smaller area. However, there are instances when digital circuits built with HV devices are required. One particular case is the implementation of a HV RC-triggered electrostatic discharge (ESD) power clamp, where a HV inverter chain and a digital latch are required. Since digital blocks cannot be reliably built with HV

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transistors, there is a need for a new HV RC-triggered protection scheme that can work without any digital circuits.

This paper presents a novel RC-triggered ESD power clamp that can be used in HV processes with limited V_{GS} voltage. The proposed circuit addresses two important shortcomings of the standard RC-triggered topology with a very simple and area efficient design: the inability to construct the reliable HV CMOS inverter driver chain required by RC-triggered protection circuits in BCD processes and the possible oscillation of the RC-triggered clamp without the use of a latching circuit. The proposed architecture is implemented in a 0.25-μm BCD CMOS process, where LDMOS drain-to-source voltage (V_{DS}) can withstand 40 V while its gate-to-source voltage (V_{GS}) should be restricted to below 5 V.

The paper is organized as follows. Section 2 provides a brief overview of the power clamp techniques used in BCD processes. Section 3 presents and discusses the RC-triggered ESD protection circuit. Section 4 details the proposed architecture, and Section 5 presents the simulation results.

2. Review of ESD protection in BCD processes

The gate-grounded NMOS transistor, shown in Figure 1, is one of the most used ESD protection elements due to its straightforward implementation [4].

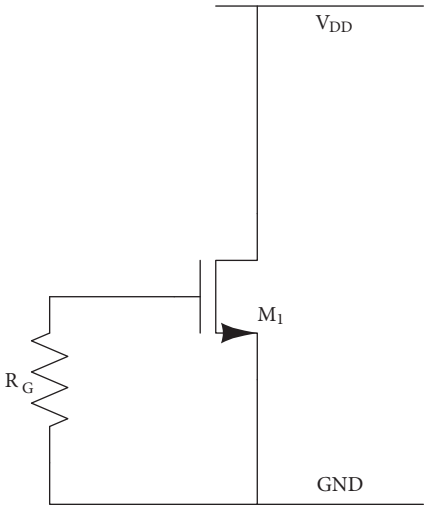

Figure 1. Gate-grounded ESD power clamp.

The protection mechanism depends on the avalanche breakdown of the NMOS, M_1. Although this is a very area-efficient protection method, it presents two important problems. First, the breakdown mechanism is not always well modeled. This requires extensive in-house modeling and iterations to achieve the required ESD performance and necessitates redesign and more iterations for any technology change or migration. Secondly, and specific to HV processes, these structures are very prone to latch-up once triggered, due to the low holding voltage of the HV NMOS transistors after the snapback [5].

Silicon-controlled rectifier (SCR) protection circuits, shown in Figure 2, are another popular method due to their high power-handling capabilities. However, they are very prone to unintended latch-up and, similarly to the gate-grounded NMOS topology, they require extensive in-house hardware verification, making reuse and migration very difficult.

As a result of the shortcomings of these two popular methods, an RC-triggered protection scheme is

a very desirable solution, as the protection mechanism works on the well-modeled transient behavior of the transistors.

Figure 3 shows a classic MOSFET-based inverter chain-driven RC-triggered ESD protection circuit. The operation of the circuit can be explained as follows. When the charge on the supply line is dissipated, the gate of the M_{BIGFET} is taken 'LOW', turning it 'OFF' and breaking the connection between the supply line and GND. The timing of the triggering circuit is achieved with a low-pass RC filter (implemented by R_1 and C_1); thus, these circuits are commonly referred to as RC-triggered ESD power clamps.

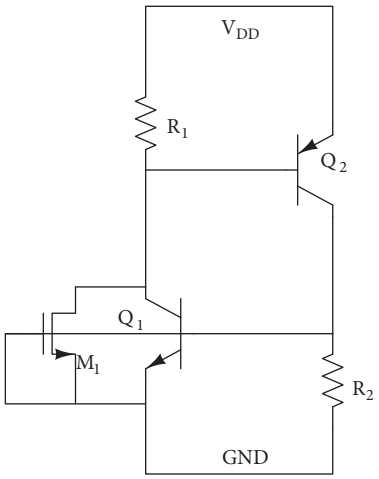

Figure 2. Silicon-controlled rectifier.

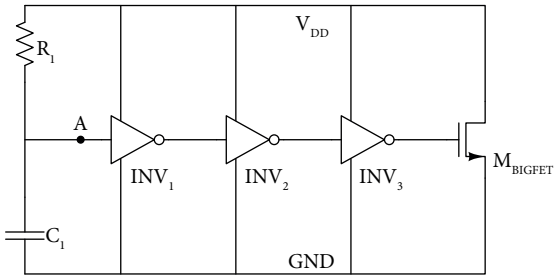

Figure 3. A typical RC-triggered ESD power clamp.

Since the operation of this circuit does not rely on the junction breakdown (as in gate-grounded NMOS), or intended latch-up (as in SCR), it can be simulated using standard circuit simulation tools with excellent accuracy. With a careful layout, the simulation results closely match the measurement results. Consequently, many of the process design kits include RC-triggered power clamps scalable to the required ESD protection level. Since optimization can be performed early in the design stage by circuit designers, they are very reliable, and they can be simulated along with the internal circuit blocks. Moreover, the design is process-independent, enabling easy modification for process changes or migration. However, like any other ESD protection element, care must be taken in the layout phase for the circuit not to suffer from parasitic resistance effects. First of all, the designer should follow the ESD design rules (which may be different from the standard design rules) provided by the factory. The designer should use an abundance of substrate vias to prevent charge leakage, as well as very wide metal wires to prevent metal snapping under large ESD discharge currents. Moreover, the ESD cell should be placed as close to the supply pads as possible (preferably right between the ground and the supply pads) to minimize the IR drop to the ESD protection elements.

3. Review of RC-triggered ESD protection circuits

The design of RC-triggered circuits in standard CMOS processes is straightforward. The time constant of the RC-discrimination circuit is adjusted with respect to the trip voltage of the first inverter to achieve M_{BIGFET} turn-on during an ESD shock. The rise time of the pulse of the human body model (HBM) ESD test is equal to 10 ns. Therefore, the timing section is adjusted so that the circuit responds to a rise of approximately 10 ns or faster while keeping the circuit turned off for a slower supply rise. Since the rise of a typical voltage supply is much slower than this value (typically larger than 1 ms), the circuit does not respond to the standard power-on, thus preventing false triggering under normal operations.

Although simple in operation, the basic RC-triggered ESD protection circuit shown in Figure 3 is prone to oscillation due to employing only one timing element [6]. This can be explained as follows: once a fast rise on the supply node is detected, M_{BIGFET} is triggered. This action rapidly starts to dissipate the ESD energy, effectively shunting the supply node to the ground. If the voltage on the supply node drops below the trip voltage of the inverters before the ESD energy is fully depleted, the M_{BIGFET} turns off, letting the supply node rise again due to the remaining ESD energy. This oscillation continues until all ESD energy is consumed, which extends the ESD discharge duration, possibly damaging the circuits to be protected.

There are various ways to circumvent this problem. A common way is to increase the time constant of the RC-discrimination circuit to keep the M_{BIGFET} ON longer. However, when used with a very fast rising power supply, this could lead to false triggering during normal operations. Another way is to separate the RC-discrimination circuit duration from the M_{BIGFET} ON duration with the use of a digital latching circuit [7], or to use multitap trigger circuits [8]. These two solutions are not suitable for BCD processes since HV digital circuits cannot be implemented reliably due to limited V_{GS} voltage values. In the proposed architecture, a novel technique based on a peak-hold circuit is employed, as will be detailed in the next section.

4. Proposed architecture

The typical HV transistor offered in the process used for this study (0.25-μm BCD from TSMC) can withstand 40-V V_{DS} voltage, whereas the gate-to-source voltage should be limited to 5 V or lower to avoid breakdown or gate oxide rupture. This limitation prevents HV transistors from being used in building certain basic functional blocks such as inverters. Since an inverter chain is required to build the standard RC-triggered ESD power clamp, a new architecture is required to effectively protect HV domain transistors.

A standard way to achieve HV protection is to stack RC-triggered circuits constructed with LV transistors or to stack diode-connected low-voltage transistors with low-voltage RC-triggered circuits, as shown in Figure 4 [9,10]. Since both methods increase the number of series devices in the discharge path, they also increase the total series resistance, thus increasing the total area of the protection circuit to achieve high ESD ratings. Therefore, they are not preferred.

The proposed architecture, as shown in Figure 5, uses only HV transistors. The operation of the circuit can be explained as follows: the RC-discrimination circuit detects the fast rise of an ESD pulse, taking the gate of the HV PMOS, M_1, low, turning it ON. Once M_1 is on, its drain is taken high, turning the HV NMOS, M_{BIGFET}, ON. Under normal operating conditions, when the supply voltage is constant, the voltage at the gate of M_1 is equal to V_{DD} (M_1 is OFF). This takes the gate voltage of M_{BIGFET} to GND, turning it OFF, which prevents any DC power dissipation under normal operation.

The circuit includes two timing elements. The first is constructed with R_1 and C_1 (in addition to the parasitic gate capacitance of M_1) to trigger the circuit under a fast-rising ESD pulse. The duration of this circuit is adjusted at around 6 ns with a 30-kΩ resistor and a 200-fF capacitor. The second timing element is constructed with D_1 and the gate oxide capacitance of the M_{BIGFET}. Any voltage built up on the gate of the M_{BIGFET} is latched by D_1, keeping the M_{BIGFET} ON until all the ESD energy is dissipated. In order to dissipate the residual charge on the gate of the M_{BIGFET}, D_2 is added to the circuit. For this implementation, the peak-hold circuit keeps M_{BIGFET} ON for approximately 600 ns for a 4000-V pulse, safely dissipating the ESD energy. With this topology, any possible oscillation is avoided without the use of digital latching circuits. It should be noted that the width of the M_{BIGFET} should be chosen with respect to the required ESD protection level. For this implementation, it was selected to be 8 mm wide to achieve Class 3A-level protection ($>$4000 V).

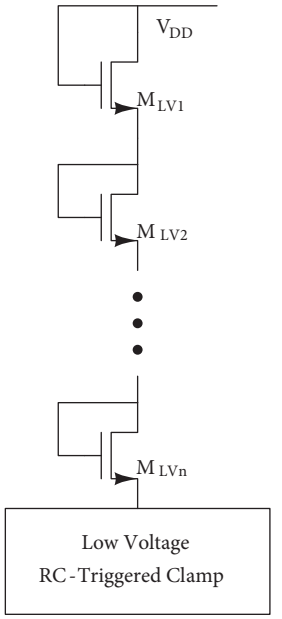

Figure 4. HV RC-triggered ESD protection with LV devices.

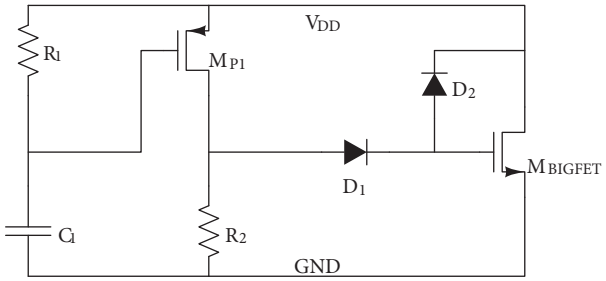

Figure 5. Schematic of the proposed circuit.

5. Simulation results

Spice simulations on the R-extracted view are performed to investigate the effectiveness of the proposed architecture. A fourth-order ESD test bench, as shown in Figure 6, is used to simulate the circuit against ESD shocks at various HBM levels. Figure 7 shows the transient simulation results of the proposed circuit at various ESD level shocks. As can be seen from the figure, the voltage on the V_{DD} line never exceeds 25 V and is dissipated fully after a very short duration. Figure 8 shows the absolute value of the V_{GS} voltage of both transistors under a 4000-V HBM shock. With optimization, the V_{GS} voltage of both transistors is kept below the maximum allowed voltage of 5 V.

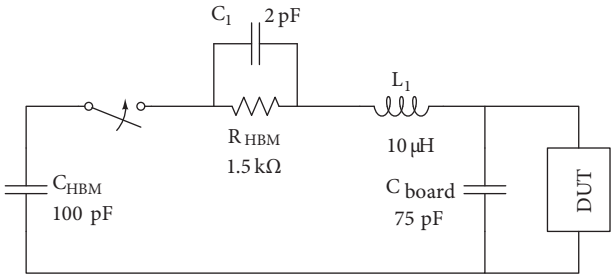

Figure 6. Fourth-order human body model ESD simulation bench.

To demonstrate the robustness of the proposed circuit against process and temperature variations, worst-case corner analyses were performed. Figure 9 shows the gate-to-source voltage of both transistors over the worst-case corner and the temperature sweep from –40 °C to 85 °C under a 4-kV ESD shock. Figure 10 shows the voltage waveforms on the V_{DD} line over the same variation process, temperature variation, and 4000-V HBM ESD shock level. As can be seen from both figures, the proposed system is very robust against process and temperature variations.

Figure 11 shows the layout of the circuit, including all components. The required area is less than 0.1

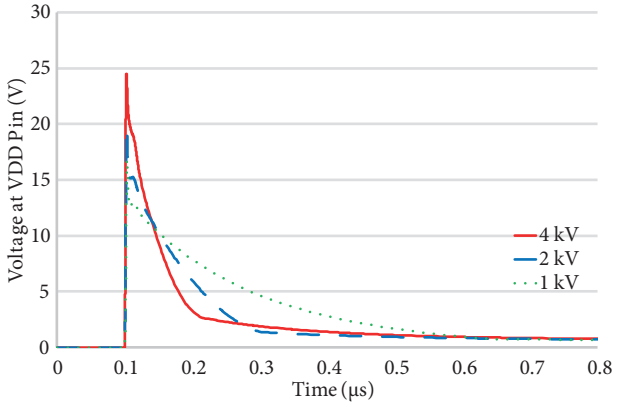

Figure 7. Voltage waveforms of the supply pin at various ESD levels.

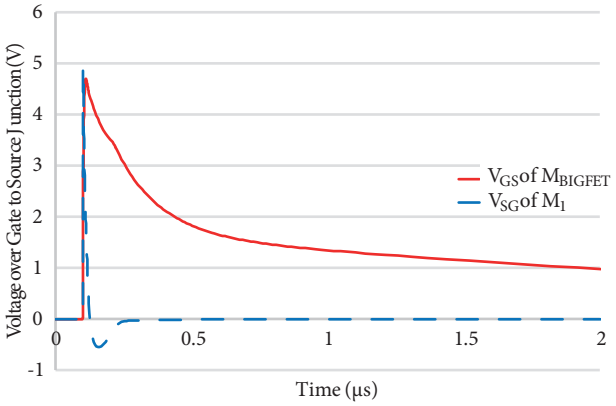

Figure 8. V_{GS} voltage of both transistors under 4 kV ESD shock.

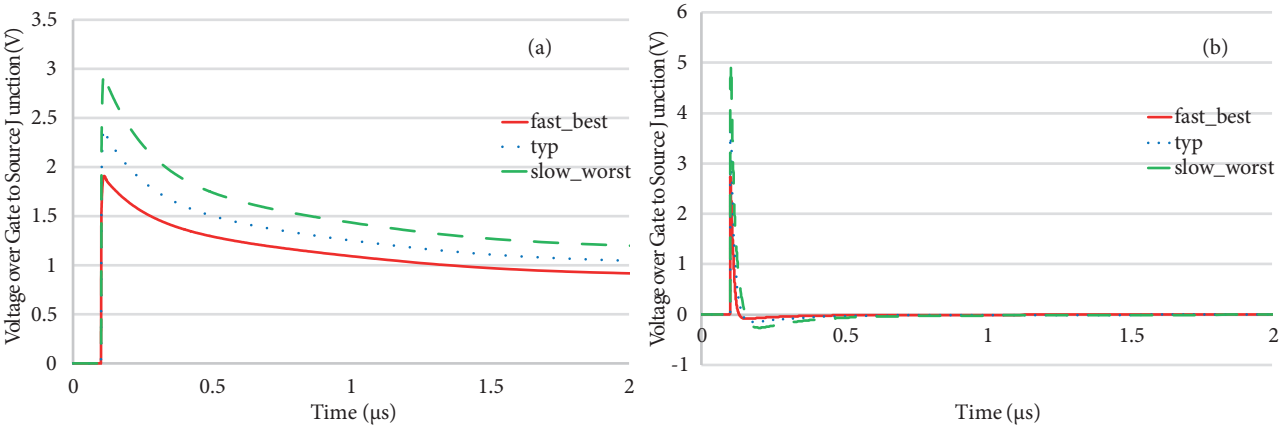

Figure 9. V_{GS} voltage of (a) M_{BIGFET} and (b) M_1 under 4-kV ESD shock over corner and temperature.

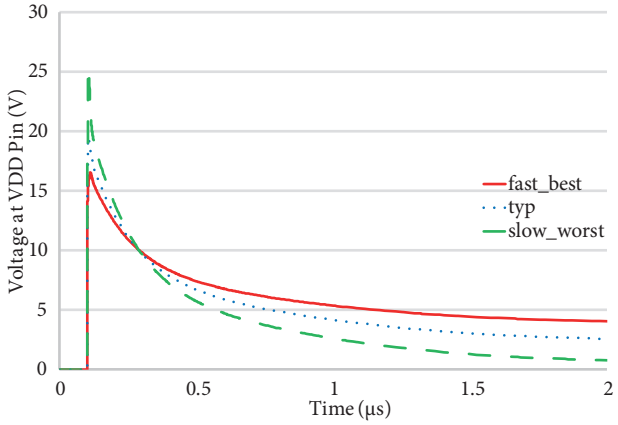

Figure 10. Voltage waveforms of the supply pin under 4-kV ESD shock over corner and temperature.

mm^2. It should be noted that the largest part of the circuit is the M_{BIGFET}. Therefore, the area will depend on the protection level required by the application. For this implementation, it was decided to build the system for a Class-3A ESD rating with a 6.4-mm-wide device. The layout size decreases dramatically with a lower ESD rating. The Table compares the specifications of this method to those of other ESD protection methods. As can

be seen from the Table, the proposed method requires a larger silicon area when compared to SCR protection. However, it does not require any hardware verification where multiple process runs, a specialized team of ESD design engineers, and semiconductor simulation tools are needed. Instead, it can be designed and simulated by using standard transient simulation tools, by circuit designers, early in the design phase.

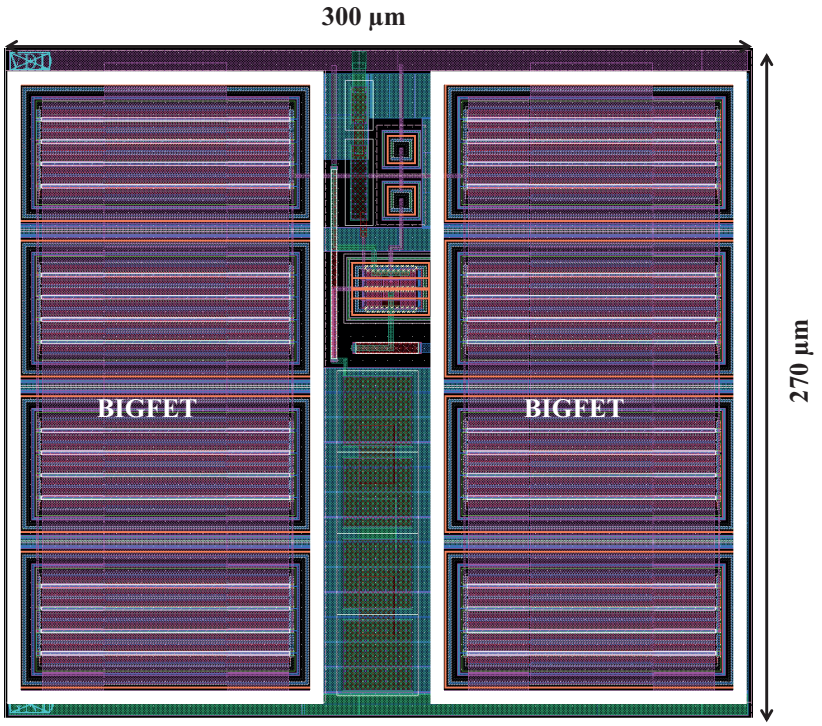

Figure 11. Layout of the ESD clamp.

Table. Comparison of ESD protection methods.

	Proposed method	Stacked low voltage [10]	SCR [11]	Gate grounded [12]
ESD level	Class 3A	Class 3A	Class 2	Class 2
Area	~ 0.1 mm^2	~ 0.1 mm^2	< 0.01 mm^2	~ 0.1 mm^2
Depends on parasitics?	No	Yes	Yes	Yes
Can be simulated with Spice?	Yes	No	No	No
Can easily be migrated to other technology nodes?	Yes	Yes	No	No

6. Conclusion

This paper presented a novel two-transistor RC-triggered ESD protection circuit for HV BCD CMOS technologies. The proposed circuit employs only two HV transistors in the active dissipation circuit and a novel peak-hold circuit separating the ON duration of the dissipation element from the RC-discrimination circuit. The circuit is implemented in a 0.25-μm BCD process offered by the TSMC. Spice simulations show that the proposed architecture can achieve protection at 4000 V with a 6.4-mm-wide NMOS device, achieving Class-3A HBM rating. The total area of the protection circuit is smaller than 0.1 mm^2. Since the circuit proposed

here does not rely on the breakdown mechanism of any active devices, Spice simulations provide very accurate results. The topology can easily be extended to other ESD levels and to other technologies without the need for extensive hardware verification.

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