Analysis and design of an interleaved current-fed high step-up quasi-resonant DC-DC converter for fuel cell applications

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Abstract: This paper proposes a current-fed quasi-resonant converter with soft switching method. Input current ripple is reduced by employing two boost circuits at the input, which makes this converter appropriate for fuel cell application. Current stress on switches is reduced because of the resonance in switches, and also, as a result of zero voltage switching in switches, switching losses will be reduced in this proposed converter. In the output, the reverse recovery problem of diodes is alleviated by zero current switching, so there is no need for fast diodes anymore. The reduction of losses improves the efficiency, and in a wide range of load, efficiency is high. Experimental results on a 1-kW prototype are provided to validate the proposed concept.

Key words: Current-fed, fuel cells, isolated boost converter, quasi-resonant DC-DC converter, zero-voltage switching

1. Introduction

These days a variety of topologies of DC-DC converters have been proposed, and they are more applicable. Different demands are considered depending on application of DC-DC converters, like high efficiency [1–3], high voltage gain [4], low voltage and/or current stress on switches [5,6], smaller size of magnetics [7], etc. A resonant converter is one kind of converter satisfying these needs [6,8–16]. These converters can operate at high frequencies [17]. Because of this, they have light weight and small size. Since the size and weight of converters is highly restricted in some applications, resonant converters are more capable. Analysis complexity is one major disadvantage of resonant converters [7,18,19].

Pulse width modulation (PWM) converters have high electromagnetic interference (EMI) and switching losses at high frequencies [20], while switching losses and EMI at high frequencies for resonant converters are low [21]. Quasi-resonant converters are a kind of resonant converters employing soft switching at zero voltage (ZVS) and/or zero current (ZCS) to reduce losses and to improve efficiency [5,6,22].

This proposed converter (Figure 1) operates in discontinuous conduction mode (DCM) to achieve minimum current stress in the turn-off switching state. Further controllability of the converter becomes easier, so this proposed converter can be controlled with a PWM method in contrast to conventional resonant converters. Consequently, the converter works at a constant frequency, reducing the EMI effect [23]. Since this converter is controlled by the PWM method, control complexity is eliminated.

Fuel cells produce unregulated and low-level voltage, and they also have low dynamics, so they require a step-up converter with low-input current ripple; because of the longer life of the fuel cell catalyst, the current

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ripple at the fuel cell output must be very low. Three basic topologies of appropriate converters were introduced in [24]. The proposed converter in [24] is a kind of current-fed PWM converter. This converter is employed by two boost circuits at the input, which work by half-period delay, so the input current ripple is reduced. Current-fed converters in general have lower transformer turns ratio than voltage-fed, which results in lower leakage inductance and copper losses and improves efficiency [24].

Many current-fed topologies have been discussed and analyzed in recent years. In [25–28], converters have hard switching and switches suffer from high voltage stress at switch turn-off. Thus, losses will increase and reduce efficiency. In [28] extra components are used to achieve ZVS, but this results in complex topology and lower efficiency.

The proposed converter, as compared to that in [24], has a lower current stress on switches (approximately half), so it has lower switching losses, but it could have more conduction losses. However, by using switches with low ON-state resistance, conduction losses of the proposed converter and that of [24] would be the same. ZCS in output diodes also alleviates the reverse recovery problem of the diodes. In this converter, like in [24], an interleaved boost circuit is used. Using interleaved boost topology requires lower transformer turns ratio. Outputs of these boost circuits are applied to the output of the converter by two high-frequency transformers. In the output two voltage doubler circuits, which are connected in series, make the DC voltage.

Leakage inductance of transformers is used for the resonant circuit. The converter works at high frequency, which causes lower weight and smaller size of transformers, inductors, and capacitors.

2. Operation principle and converter analysis

The proposed converter circuit is shown in Figure 1. Input boost circuits consist of inductance $L_{B1}$ and $L_{B2}$, and switches $S_1$ and $S_2$. Leakage inductance of transformers in the primary side is modeled as $L_{k1}$ and $L_{k2}$. Capacitors $C_1$ and $C_2$ with leakage inductances $L_{k1}$ and $L_{k2}$ provide the resonant circuits, respectively. Active clamp circuits are made by $C_2$ and $C_4$ and switches $S_2$ and $S_4$, respectively. In the secondary side of the transformers, diodes $D_1$, $D_2$ and $D_3$, $D_4$ work as a half-bridge rectifier, providing two voltage doubler circuits with capacitors $C_{O1}$, $C_{O2}$, $C_{O3}$, and $C_{O4}$, which are connected in series at the output. Voltage polarization of capacitors $C_1$ and $C_2$, current direction of switches $S_1$ and $S_2$, and inductor $L_{B1}$ are shown in Figure 1. The same components of the second leg have the same voltage polarization and current direction as in the first leg.

In this converter, the resistance of switches is neglected. Because of ZCS on the output diodes, fast diodes are not necessary. Moreover, $R_L$ is the candidate for the load resistance. $N_1$ and $N_2$ are the primary and secondary turn ratio of transformer $T_1$, respectively, and $N_3$ and $N_4$ for transformer $T_2$. The turn ratios

![Figure 1. Proposed converter.](image-url)
of these two transformers are the same, so is defined as. \( f_s \) and \( f_r \) are switching and resonant frequencies, respectively.

The operation of the proposed converter has twelve intervals. The first and second six intervals are the same, so here the first six intervals will be described. Important currents and voltage curves are shown in Figure 2 and circuit diagrams are shown in Figure 3. At the time before \( t_0 \), switches \( S_2 \) and \( S_4 \) are turned on. Inductances \( L_{B1} \) and \( L_{B2} \) are large enough to alleviate input current ripple, so it is assumed that the input current has a constant value of \( I_{in} \). Furthermore, it is assumed that the voltage of \( C_2 \) and \( C_4 \) has a constant value of \( V_C \).

![Figure 2. Important waveforms of proposed converter.](image-url)
1) **Interval 1** \([t_0 - t_1]\)

At \(t_0\), \(S_2\) turns off and the difference of \(I_{LB1}\) and the transformer \(T_1\) current flows through the antiparallel diode of switch \(S_1\). As long as this current flows, voltage across \(S_1\) is zero and gate pulse can be applied to achieve ZVS. The current of transformer \(T_2\) is zero, but the current of \(S_3\) remains \(I_{LB2}\) in the entire interval and the power supply charges the inductor \(L_{B2}\).

At the output, diodes \(D_2\), \(D_3\), and \(D_4\) are turned off. This interval will finish when the reverse current of \(S_1\) decreases to zero.

2) **Interval 2** \([t_1 - t_2]\)

At \(t_1\), the current of switch \(S_1\) changes its direction and flows through the switch because \(S_1\) was turned on in the previous interval. \(I_{in}\) circulates through \(S_1\) and the source, and \(V_{in}\) charges input inductor \(L_{B1}\). By applying voltage \(V_1 = V_{O1}/2n\) via transformer \(T_1\), primary winding to \(C_1\) and \(L_{k1}\) in two last intervals, \(i_{lk1}\), decreases to zero. This interval will finish when \(i_{lk1}\) reaches zero. In the output \(D_3\) is conducting. Thus:

\[
-i_1 = -\frac{V_{o1}/2n - V_{C1}'}{L_k}d_1T_S, \tag{1}
\]

\[
d_1T_S = t_2 - t_0, \tag{2}
\]

where \(V_{C1}'\) is the voltage of capacitor \(C_1\) at time \(t_0\).

3) **Interval 3** \([t_2 - t_3]\)

At \(t_2\), the current of transformer \(T_1\) changes its direction and the voltage of output capacitor \(C_{O2}\) is reflected via this transformer to the primary side, and \(C_1\) and \(L_{k1}\) make resonance. During this interval, as a result of \(V_{in}\) across \(L_{B1}\), the current of the input inductance is rising. Because of changing the direction of \(i_{lk1}\) in this interval, the direction of the secondary current is also changed, so in the output doubler circuit, \(D_2\) is conducting and supplies output capacitor \(C_{O2}\). In these two last intervals, the second leg operates the same as in the first interval.

4) **Interval 4** \([t_3 - t_4]\)

At \(t_3\), \(S_3\) turns off and the difference of \(I_{LB2}\) and the current of transformer \(T_2\) flows through antiparallel diode of switch \(S_4\) and charges \(C_4\). At the beginning of this interval, the parasitic capacitor of \(S_4\) and \(S_3\) is discharged and charged to \(V_{in}/(1 - D)\). As long as the current flows through the body diode of \(S_4\), voltage across \(S_4\) is zero and the gate pulse can be applied to achieve ZVS. In the output, \(D_2\) and \(D_3\) are conducting. This interval will finish when the reverse current of \(S_4\) reaches zero.

5) **Interval 5** \([t_4 - t_5]\)

When the current of the antiparallel diode of \(S_4\) reaches zero, its direction changes, and it flows through switch \(S_4\), which has been turned on in the previous interval. The current of transformer \(T_2\) is rising just like in the previous interval. In these two later intervals, the constant current of \(L_{LB2}\) flows through transformer \(T_2\) and charges \(C_3\). The current of capacitor \(C_4\) circulates through transformer \(T_2\). This interval finishes by removing the pulse gate of \(S_4\). In these two last intervals, the second leg operates the same as in interval 3. For this interval:

\[
d_2T_S = t_5 - t_2, \tag{3}
\]

\[
i_{lk}(t_5) = \frac{V_{o2}/2n - V_{C1}'}{\sqrt{T_{L2}/C_1}} \sin(\omega_r d_2T_S) = 0, \tag{4}
\]
\[ d_2 T_S = \pi \sqrt{L_k C_1}, \tag{5} \]

where \( V_2 = V_{O2}/2n \) is voltage of capacitor \( C_{O2} \), reflected to the primary side of the transformer.

6) **Interval 6 \([t_5 - t_6]\)**

This interval will begin when the current of transformer \( T_1 \) reaches zero. Capacitor \( C_1 \) and inductor \( L_{k1} \) transfer their energy to the output, and consequently the voltage across transformer \( T_1 \) reaches zero. However, the current of \( S_1 \) remains \( I_{LB1} \) in the entire interval and the power supply charges inductor \( L_{B1} \). Based on the diagrams shown in Figure 2:

\[ d_3 T_S = t_9 - t_5 = DT_S - d_1 T_S - d_2 T_S, \tag{6} \]

and, by applying the volt-second law to the transformer winding:

\[ d_1 V_1 + d_3 V_3 = d_2 V_2, \tag{7} \]

\[ V_3 = \frac{d_2 V_2 - d_1 V_1}{d_3}. \tag{8} \]

At the output, diodes \( D_1 \) and \( D_2 \) are turned off because the secondary current is zero. At time \( t_3 \) the current of transformer \( T_2 \) rises linearly from 0 until \( t_6 \) reaches \( t_1 \). Thus:

\[ i_1 = \frac{V_C - V_{O3}/2n}{L_k} (1 - D)T_s, \tag{9} \]

\[ (1 - D) T_s = t_6 - t_5. \tag{10} \]

\( V_C \) is the voltage of the clamp capacitor and \( V_{O3}/2n \) is the voltage of \( C_{O3} \) on the output, which was reflected to the primary side of the transformer, which is equal to \( V_1 \), and \( DT_s \) is duty cycle of switch \( S_1 \).

3. **Theoretical analysis**

3.1. **Voltage gain**

Here it is assumed that the voltage of capacitors \( C_1, C_2 \), output capacitors, and input current \( I_{in} \) are constant. According to proposed converter in Figure 1, by applying KCL to node “a”, the average current of \( C_1, C_2 \), and \( L_k \) is zero.

\[ \langle i_{k1} \rangle + \langle i_{C1} \rangle + \langle i_{C2} \rangle = 0 \tag{11} \]

Here, “\( \langle \bullet \rangle \)” means the average value of “\( \bullet \)”. In the steady state, the average current of the capacitors is zero; that is:

\[ \langle i_{C1} \rangle = \langle i_{C2} \rangle = 0, \tag{12} \]

and therefore:

\[ \langle i_{k1} \rangle = 0. \tag{13} \]

However, during time \( (1 - D) T_s = t_6 - t_4 \), by applying KCL in node “b”:

\[ i_{C1} + I_{in} = i_{LK}. \tag{14} \]
Here $I_{in}$ is the average input current. Switch $S_2$ is in series with capacitor $C_2$ ($i_{C_2}-i_{S_2}$) so from Eq. (13) its average current is zero. From Figure 2 during time $(1-D)T_s$, the average current of $i_{lk}$ is equal to $I_{in}$, and then:

$$\frac{1}{2}i_1(1-D)T_S = I_{in}(1-D)T_S,$$

(15)

$$i_1 = 2I_{LB} = I_{in}.$$ 

(16)

By applying KVL:

$$\langle V_{in} \rangle = \langle V_{LB1} \rangle + \langle V_{T1} \rangle + \langle V_{Lk1} \rangle + \langle V_{C1} \rangle.$$ 

(17)

In the steady state the average voltage of the inductors and the windings of the transformer are zero, and so:

$$\langle V_{in} \rangle = \langle V_{C1} \rangle.$$ 

(18)

As shown in Figure 3 at time $t_9$ to $t_{12}$ the current $I_{in}$ flows through $C_1$ and then the current of $C_1$ jumps to $i_1$; after that it decreases almost linearly to zero. Simultaneously the voltage of $C_1$ during time $t_9$ to $t_{12}$ increases linearly and after that it has resonance and reaches its peak value at $t_8$. Its minimum occurs at $t_{11}$ and it is constant to $t_3$.

Voltage of $C_1$ increases linearly from $t_9$ to $t_{12}$. The time interval between $t_6$ and $t_8$ is too short, and consequently it can be assumed that in this interval voltage of $C_1$ is constant. From Eq. (18) it can thus be said that:

\[ \langle V_{in} \rangle = \langle V_{C1} \rangle. \]
\[
\Delta V_{C1} = \frac{I_{in}}{C_1} (1 - D)T_S, \tag{19}
\]

\[
V'_C = V_{C1} (t_0) = V_{in} + \frac{\Delta V_{C1}}{2} = V_{in} + \frac{I_{in}}{2C_1} (1 - D)T_S. \tag{20}
\]
From Figure 4 and by applying volt-second product equations on output capacitors, relations among $V_{O1}$, $V_{O2}$, and $V_O$ can be easily obtained as follows [29]:

$$V_{O1} = (1 - D + d_1)V_O/2,$$

$$V_{O2} = (D - d_1)V_O/2.$$  

(21) 

(22)

$V_C$ can be represented as:

$$V_C = \left( \frac{D}{1 - D} \right)V_{in}.$$  

(23)

From Eqs. (1), (9), (20), (21), and (23)

The average current of each output diode is equal to the output current, because the average current capacitors are zero. Thus:

$$I_O = \frac{1}{2}i_{D2(peak)}(1 - D + d_1).$$  

(25)

From Figure 2 and Eq. (16):

$$i_{D2(peak)}n = i_1 = I_{in}. $$  

(26)

By using Eqs. (25) and (26), the output current can be obtained as:

$$I_O = \frac{I_{in}}{2n}(1 - D + d_1).$$  

(27)

By assuming that the converter is lossless, it can be said that:

$$M = \frac{V_O}{V_{in}} = \frac{I_{in}}{I_O} = \frac{2n}{1 - D + d_1},$$  

(28)

and so if the transformers are assumed to be ideal, leakage inductance and $d_1$ can be neglected and ideal voltage gain will be as follows:

$$M = \frac{2n}{1 - D}.$$  

(29)
By using Eqs. (9), (25), and (26), the output current can be obtained as:

\[
I_O = \left[ \frac{D - d_1}{1 - D} \right] \frac{V_{in}}{2nL_{Lk}} \cdot (1 - D)(1 - D + d_1)T_S = \frac{V_O}{R_L}
\]  

(30)

and:

\[
M = \frac{D}{\left( \frac{2nL_{Lk}}{R_L} \right) + (D - d_1)\frac{1 - D}{2n}}.
\]  

(31)

### 3.2. Input current ripple

The current of inductances \(L_{B1}\) and \(L_{B2}\) and input current are shown in Figure 5. The average currents of \(L_{B1}\) and \(L_{B2}\) are \(I_{LB1}\) and \(I_{LB2}\), respectively, so:

\[
I_{LB1} = I_{LB2} = \frac{1}{2}I_{in}.
\]  

(32)

Assume that:

\[
L_{B1} = L_{B2} = L_B.
\]  

(33)

\(I_{in}\) is the average of the input current. The current ripple of each inductance is obtained as in the following relation:

\[
i_2 - i_1 = \frac{V_{in}DT_S}{L_B},
\]  

(34)

and for \(i_1\) and \(i_2\) it can be said that:

\[
i_1 = \frac{I_{in}}{2} - \frac{V_{in}DT_S}{2L_B},
\]  

(35)

\[
i_2 = \frac{I_{in}}{2} + \frac{V_{in}DT_S}{2L_B}.
\]  

(36)

To achieve input current ripple, the maximum and minimum of the input current should be calculated at \(t_6\) and \(t_9\). At time \(t_6\) the value of \(I_{LB2}\) is \(i_1\), so:

\[
i_{in}(t_6) = i_1 + \frac{V_{in}T_S}{2L_B} = \frac{I_{in}}{2} - \frac{V_{in}T_S}{2L_B}(D - 1),
\]  

(37)

and at time \(t_9\):

\[
i_2 + \frac{V_{in}T_S}{L_B}(D - 0.5) = \frac{I_{in}}{2} + \frac{V_{in}T_S}{2L_B}(3D - 1).
\]  

(38)

Thus, the input current ripple is obtained as:

\[
\Delta I_{in} = i_{in}(t_9) - i_{in}(t_6) = \frac{V_{in}T_S}{L_B}(2D - 1).
\]  

(39)

The input current ripple will be zero if \(D = 0.5\).
3.3. ZVS conditions

According to interval 4, when switch $S_3$ goes off the current of input inductance $L_{B1}$ flows through the body diode of $S_4$, and the parasitic capacitors of $S_4$ and $S_3$ are discharged and charged, respectively. The following condition should thus be satisfied to ensure ZVS for $S_4$:

$$\frac{1}{2}L_B I_{LB}^2 = \frac{1}{2}L_B \left(\frac{I_{in}}{2}\right)^2 > C_{OSS} \left(\frac{V_{in}}{1-D}\right)^2.$$  \hspace{1cm} (40)

$C_{OSS}$ is the parasitic capacitor of the switches. This shows that ZVS for switches $S_2$ and $S_4$ is achieved for all load ranges. At $t_6$ when $S_4$ turns off, the difference of $i_{LB2}$ and $i_{ik2}$ flows through the body diode of $S_3$. Thus:

$$-i_{S3}(t_6) = i_{ik2}(t_6) - i_{LB2}(t_6) = i_1 - I_{LB2} = \frac{I_{in}}{2}.$$  \hspace{1cm} (41)

The current of the body diode of $S_2$ is $I_{in}/2$, and the ZVS condition is obtained the same as for the switch.

3.4. Boundary between the CCM and DCM

As mentioned before, the proposed converter operates in DCM, but the boundary between DCM and continuous conduction mode (CCM) for the first leg is at $t_5$, where the current of leakage inductance reaches zero. If the duty cycle is longer than $t_5$, the proposed converter goes to DCM, and so the boundary duty ($D_b$) cycle is obtained as:

$$D_b = \frac{t_5 - t_0}{T_S} = d_1 + d_2.$$  \hspace{1cm} (42)

4. Comparison and experimental and simulation results

A comparison between the L-type half-bridge converter and isolated boost converter that was proposed in [20] was done in [20] with the following properties: $P_o = 1$ kW, $V_{in} = 26-50$ V, $V_o = 400$ V, $\Delta I_{in} = 10\%$, $f_s = 50$ kHz.

In this paper, a comparison among the proposed converter, L-type half-bridge converter, and proposed converter of [24] is presented in the Table, and simulations and experimental results are shown in Figures 6 and 7, respectively. All three converters have the same specifications, except that in the proposed converter the switching frequency and output voltage ripple are 100 kHz and 0.2%, respectively.
Table. Comparison among proposed converter in [24], L-type half-bridge converter, and proposed converter.

<table>
<thead>
<tr>
<th>Component</th>
<th>Design items</th>
<th>Conventional L-type HB converter</th>
<th>Proposed converter in [20]</th>
<th>Proposed converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch</td>
<td>Vpk</td>
<td>140 V</td>
<td>90 V</td>
<td>Main 137 V</td>
</tr>
<tr>
<td></td>
<td>Vstress</td>
<td>140 V</td>
<td>90 V</td>
<td>Clamp 150 V</td>
</tr>
<tr>
<td></td>
<td>Ipk</td>
<td>Main 60 A</td>
<td>51 A</td>
<td>Main 44 A</td>
</tr>
<tr>
<td></td>
<td>Istress</td>
<td>Main 60 A</td>
<td>51 A</td>
<td>Main 16 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clamp 35 A</td>
<td>Clamp 15 A</td>
<td>Clamp 15 A</td>
</tr>
<tr>
<td></td>
<td>Po/(Vpk Ipk q)</td>
<td>0.037</td>
<td>0.054</td>
<td>0.06</td>
</tr>
<tr>
<td>Diode</td>
<td>Vpk</td>
<td>400 V</td>
<td>208 V</td>
<td>200 V</td>
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<tr>
<td></td>
<td>Ipk</td>
<td>11 A</td>
<td>16 A</td>
<td>D1 12 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D2 11.4 A</td>
</tr>
<tr>
<td></td>
<td>Po/(Vpk Ipk q)</td>
<td>0.056</td>
<td>0.15</td>
<td>0.21</td>
</tr>
<tr>
<td>Transformer</td>
<td>Vrms</td>
<td>76 V</td>
<td>36.8 V</td>
<td>34 V</td>
</tr>
<tr>
<td></td>
<td>Irms</td>
<td>15 A</td>
<td>16.2 A</td>
<td>16.4 A</td>
</tr>
<tr>
<td></td>
<td>Vrms</td>
<td>265 V</td>
<td>92.2 V</td>
<td>85.6 V</td>
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<tr>
<td></td>
<td>Irms</td>
<td>4.3 A</td>
<td>6.42 A</td>
<td>6.5 A</td>
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<tr>
<td></td>
<td>KVA</td>
<td>1140 VA</td>
<td>590 VA 2</td>
<td>555 VA 2</td>
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<tr>
<td>Output capacitor</td>
<td>Capacitance</td>
<td>5.5 µF</td>
<td>7 µF × 4</td>
<td>7 µF × 4</td>
</tr>
<tr>
<td></td>
<td>Vpk</td>
<td>400 V</td>
<td>139 V</td>
<td>C1 89 V</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>C2 112 V</td>
</tr>
<tr>
<td></td>
<td>CV2(PU)</td>
<td>1</td>
<td>0.54</td>
<td>0.32</td>
</tr>
<tr>
<td>Input inductor</td>
<td>Inductance</td>
<td>17 µH × 2</td>
<td>13 µH × 2</td>
<td>50 µH × 2</td>
</tr>
<tr>
<td></td>
<td>Irms</td>
<td>25 A</td>
<td>25 A</td>
<td>16 A</td>
</tr>
<tr>
<td></td>
<td>LF(PU)</td>
<td>1</td>
<td>0.76</td>
<td>1.2</td>
</tr>
<tr>
<td>Auxiliary capacitor</td>
<td>Capacitance</td>
<td>7 µF</td>
<td>14 µF × 2</td>
<td>14 µF × 2</td>
</tr>
<tr>
<td></td>
<td>Vpk</td>
<td>140 V</td>
<td>63 V</td>
<td>54 V</td>
</tr>
<tr>
<td></td>
<td>CV2(PU)</td>
<td>1</td>
<td>0.81</td>
<td>0.60</td>
</tr>
<tr>
<td></td>
<td>Switching losses (PU)</td>
<td>1 Main 0.86</td>
<td>0.55 Main 0.55</td>
<td>Clamp 0.27</td>
</tr>
</tbody>
</table>

According to the Table, the peak voltage of the proposed converter and the L-type half-bridge converter are the same and are double the peak voltage of the proposed converter in [24]. Thus, MOSFETs chosen for the proposed converter would have more R\text{on}, and conduction losses in the proposed converter will be greater than those of the proposed converter in [24]. However, because of the resonance nature, voltage stress at switch S_1 is half in comparison with the proposed converter in [24], which causes very lower switching losses. Peak current of the main switch of the proposed converter is lower than that of the other two converters. This difference for clamp switch and current stress of the switches in the proposed converter is very high, so in the proposed converter the switching losses are much lower than the others. Because of the resonance nature, current stress is much lower than the current peak in the main switch. The reverse voltage of the diodes in the proposed converter is approximately the same as that of the proposed converter in [24]. The utilization factor has been improved for the switches and diodes in the proposed converter. Input inductors in the proposed converter are...
Figure 6. Simulation waveforms of proposed converter: (a) $i_{lk1}$ and $i_{lk2}$, 5 A/div; (b) $i_{S1}$ and $i_{S1}$, 10 V/div; (c) $i_{D1}$ and $i_{D2}$, 2.5 A/div; (d) $i_{LB1}$ and $i_{LB2}$, 2.5 A/div; (e) $I_{in}$, 5 A/div.

larger and their energy is greater than in the others, but the output and auxiliary capacitors are the same and their energy in the proposed converter is lower than in the others.

For switching losses, it is assumed that the base losses are the switching losses of the main switch of the L-type half-bridge converter, so other switches losses are presented as per unit. According to the Table, the switching losses of the proposed converter in [24] are two and six times greater than those of the clamp and main switch in the proposed converter. In the L-type converter the switching losses of the main and clamp switches are about twelve and two times greater than those of the same switches in the proposed converter.

In this proposed converter leakage inductance of transformers is $L_k = 2 \mu H$, and other component values are mentioned in the Table. Figure 7a shows the current of switches $S_1$ and $S_2$, and the turning on of ZVS is shown here. As shown in Figure 7a, because of the resonance nature in switch $S_1$, current stress is much lower than the current peak, as mentioned before. In Figure 7b the current of the leakage inductance of the transformers is shown, and it is clear that the proposed converter works in DCM. In Figure 7c the current of the output diodes and the turning on and off of ZCS are shown. Because of the ZCS in the output diodes, the reverse recovery problem of these diodes is alleviated and there is no need for fast diodes anymore. In Figure 7d the current of input inductors and input current are shown, respectively. According to this figure, the current
of input inductors by half-period time delay causes lower ripple at the input current. Voltage gain against duty cycle for some leakage inductance values is plotted in Figure 8. Here the boundary duty cycle between DCM and CCM is about 0.4. According to Figure 8, the proposed converter can be controlled by the duty cycle in both DCM and CCM. The efficiency of the proposed converter and the converter in [24] is plotted in Figure 9. Maximum efficiency of the proposed converter is 97.9%, which occurs at 320 W output power, and full load efficiency is 95.7%.

5. Conclusion
In this paper an interleaved quasi-resonant current-fed converter is proposed and compared with two other converters. Voltage and current stress of the proposed converter are lower than those of the others and so switching losses in the turn-off state are improved. Because of ZVS in the turn-on state, it has minimum switching losses. As a result of ZCS in the output diodes, the reverse recovery problem is alleviated and diode switching losses are reduced. Because of this reduction of losses, efficiency is improved. A major disadvantage of resonant converters is their control complexity. In this paper, the proposed converter works in DCM, so, as is proved before, it can be controlled by the PWM method and therefore its control complexity is reduced.
Figure 8. Output voltage against duty cycle for various leakage inductances.

Figure 9. Efficiency at different output power.

References


